Marching to the Beat of Moore's Law

Yan Borodovsky

Portland Technology Development
Intel Corporation
Hillsboro, Oregon, USA

" The Definition of "Moore's Law" has come to refer to almost anything related to the semiconductor industry that when plotted on semi-log paper approximates a straight line"

Gordon Moore
Plenary Talk
February 19, 1995
E-Beam, X-Ray, EUV and I-beam Lithography for Manufacturing V
Santa Clara, Ca USA

Moore's 1965 insight:

" I wanted to get across the idea that integrated circuits were a way to make electronics cheap.

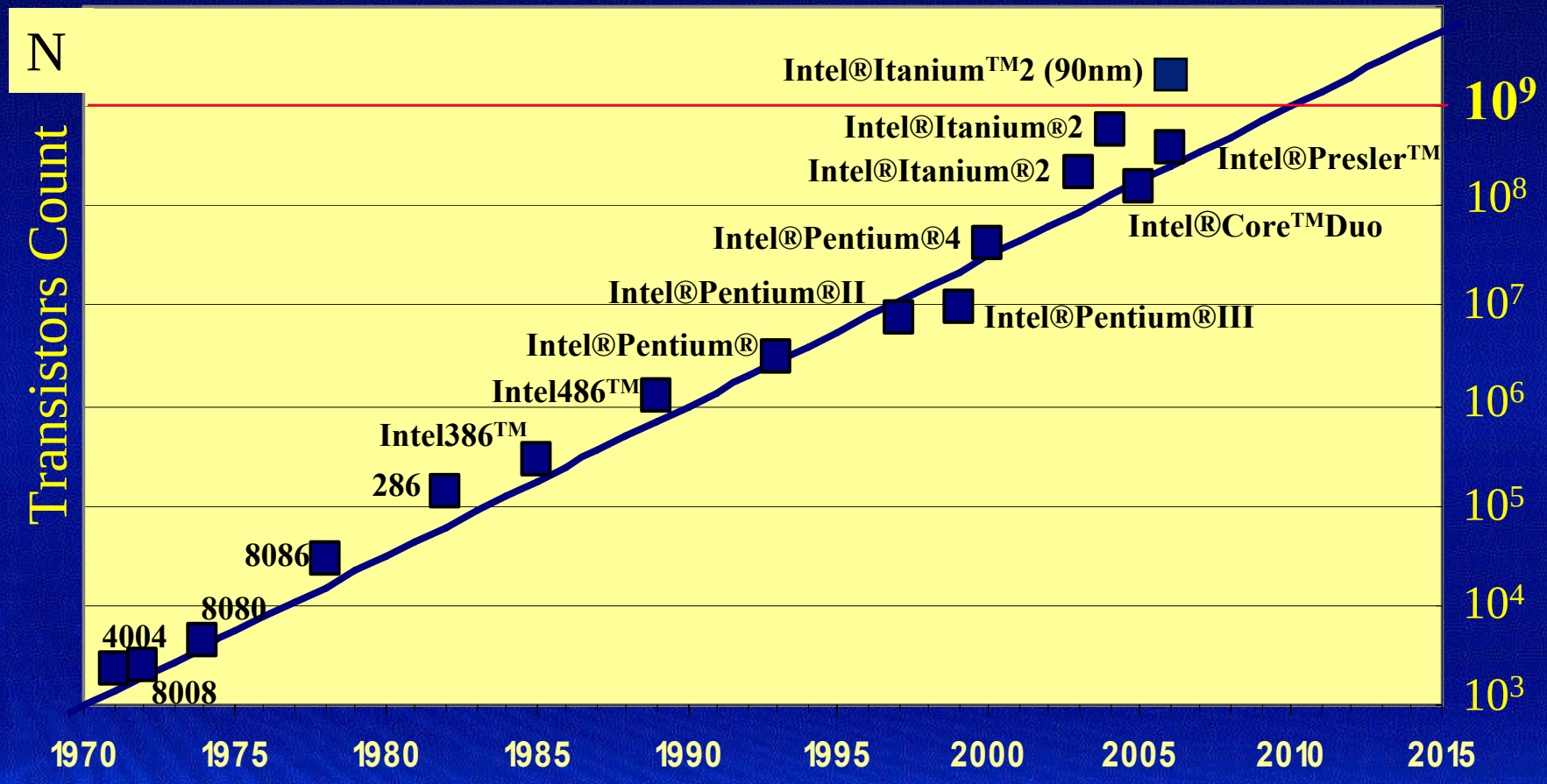
You could see the technology was going to let you make more complex things and the costs were going to go down.

That was really the message I wanted to get across."

Gordon Moore
San Jose Mercury News
April 2, 2005

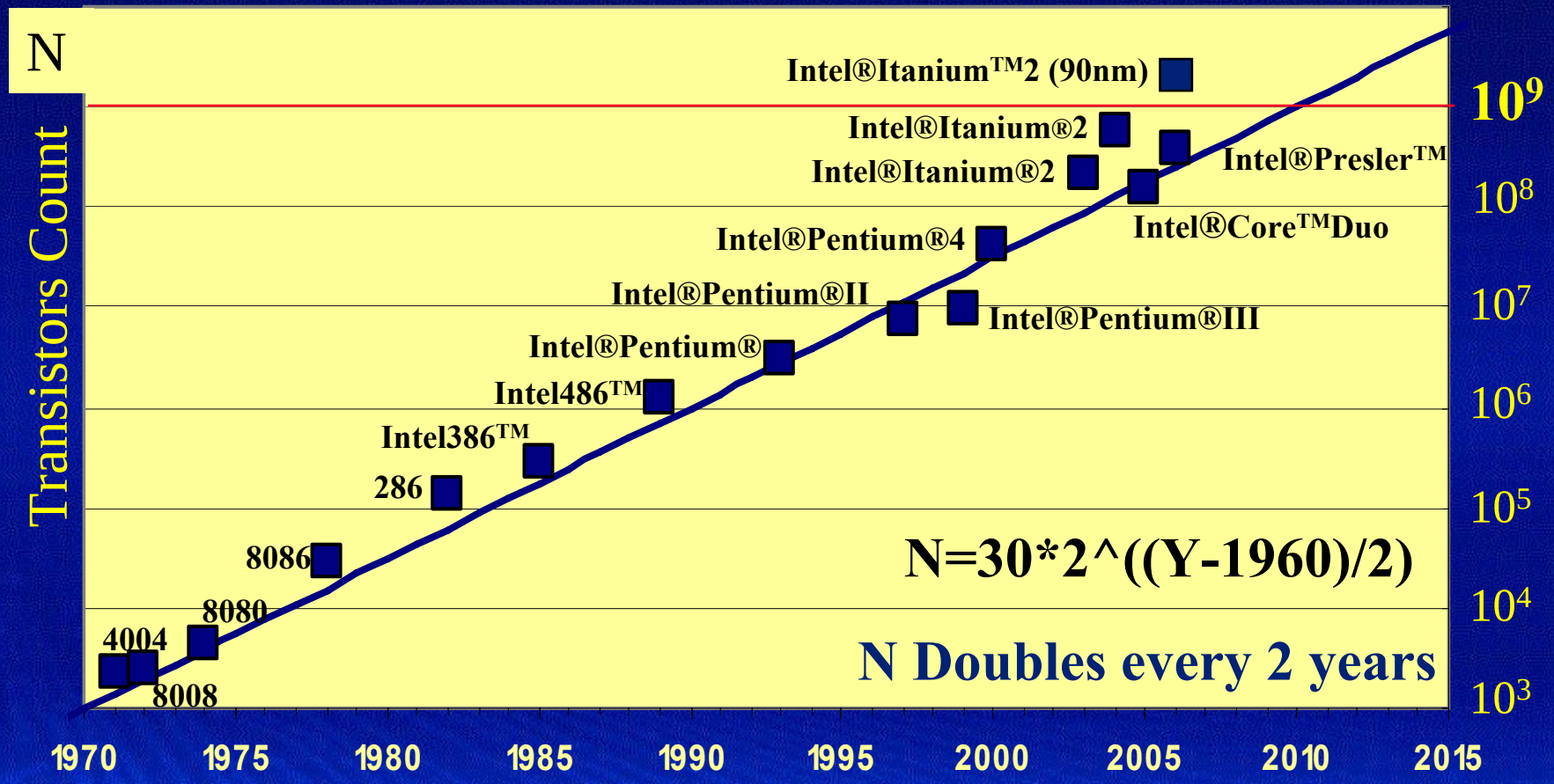
Exponential Complexity Growth

Intel Microprocessors Complexity 1971 -2006



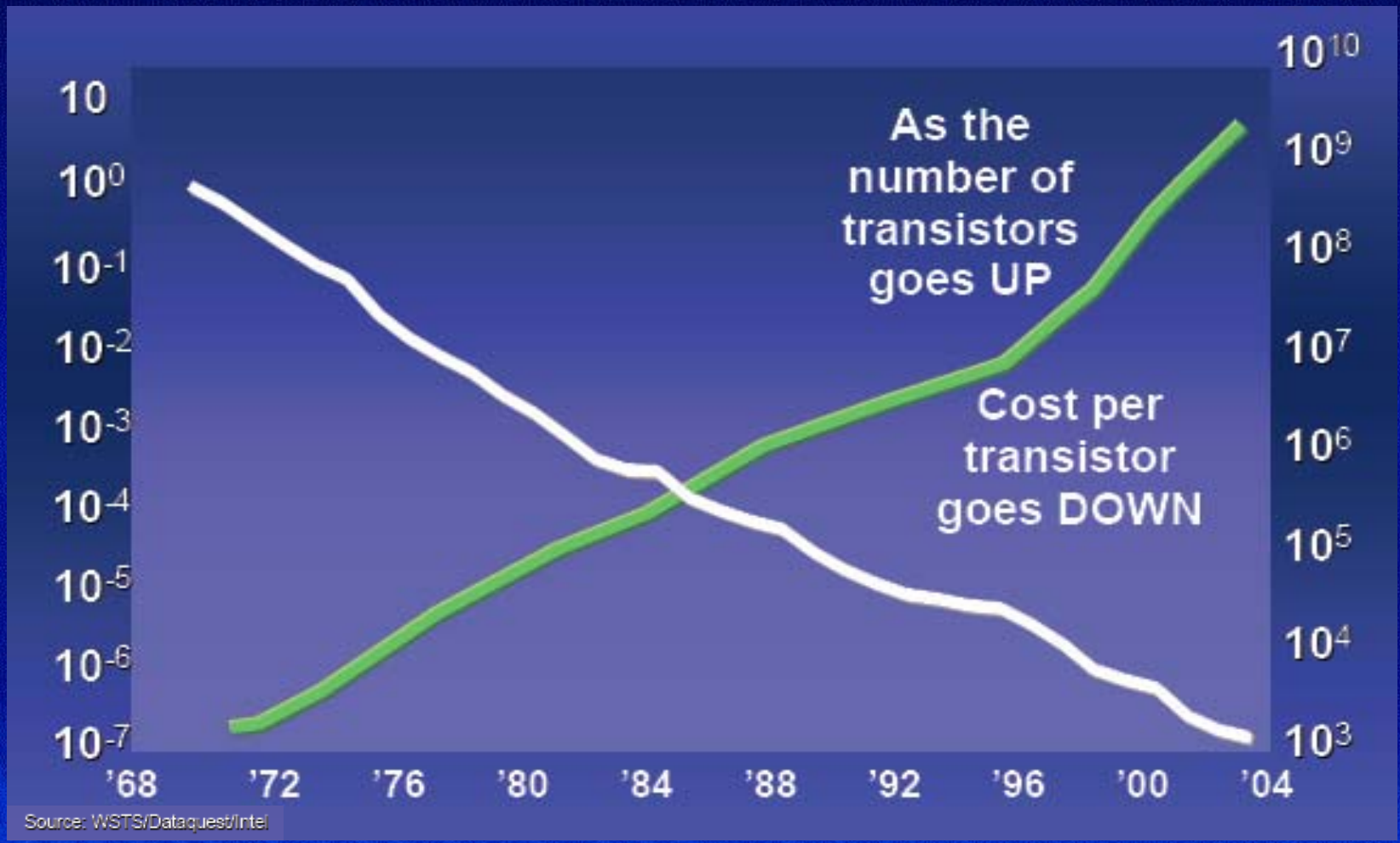
Exponential Complexity Growth

Intel Microprocessors Complexity 1971 -2006



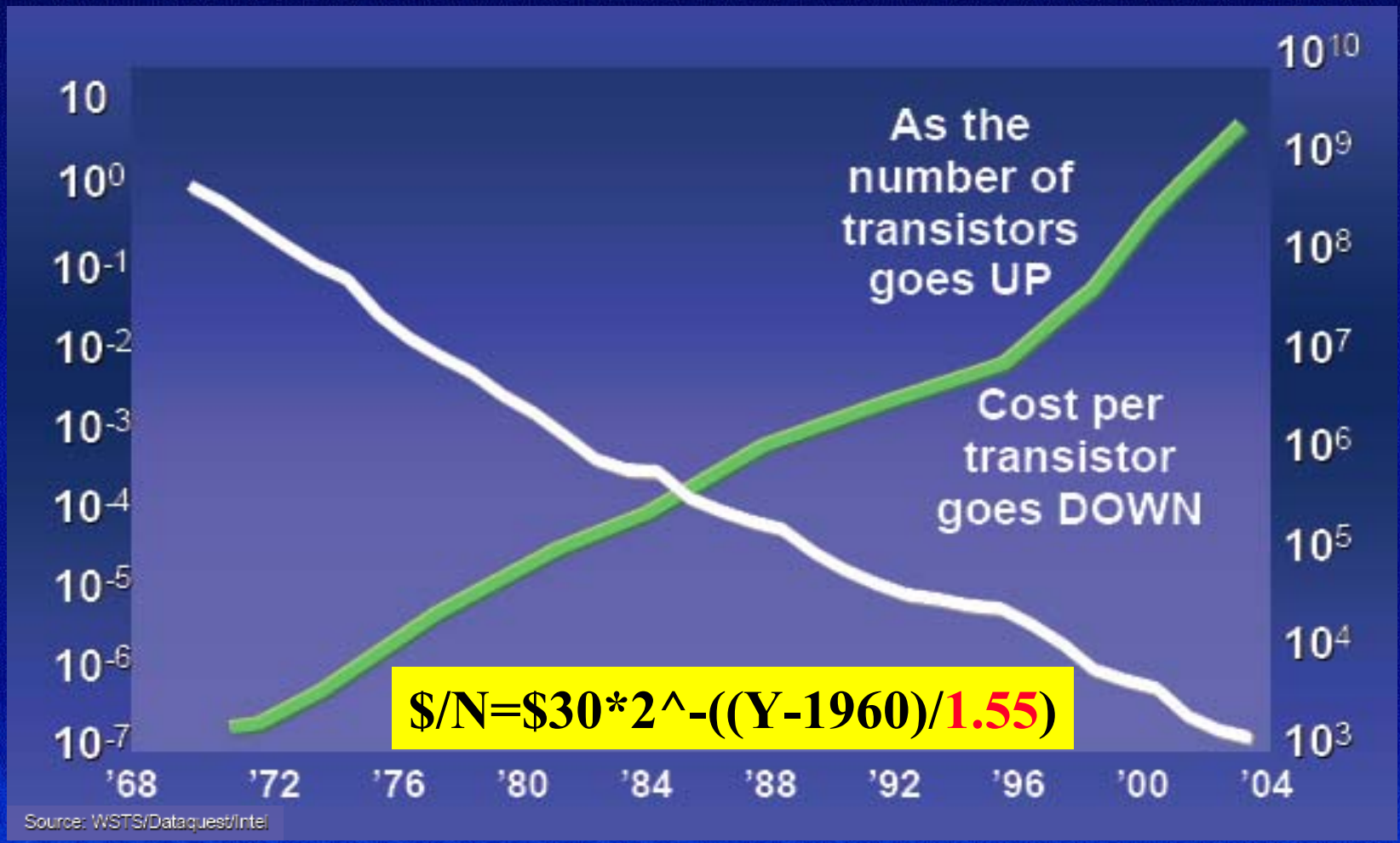
Exponential Cost Reduction

Cost per Transistor



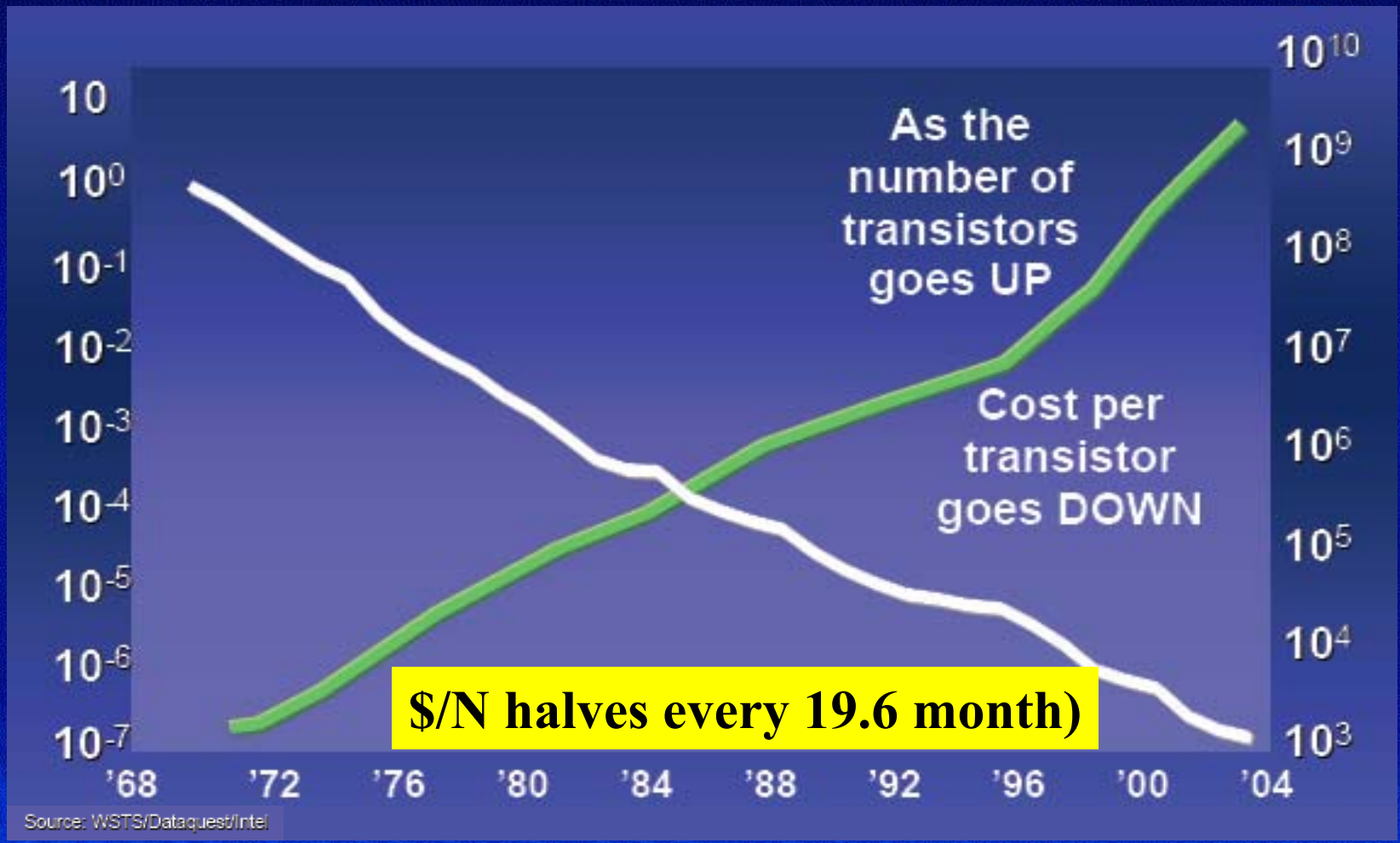
Exponential Cost Reduction

Cost per Transistor



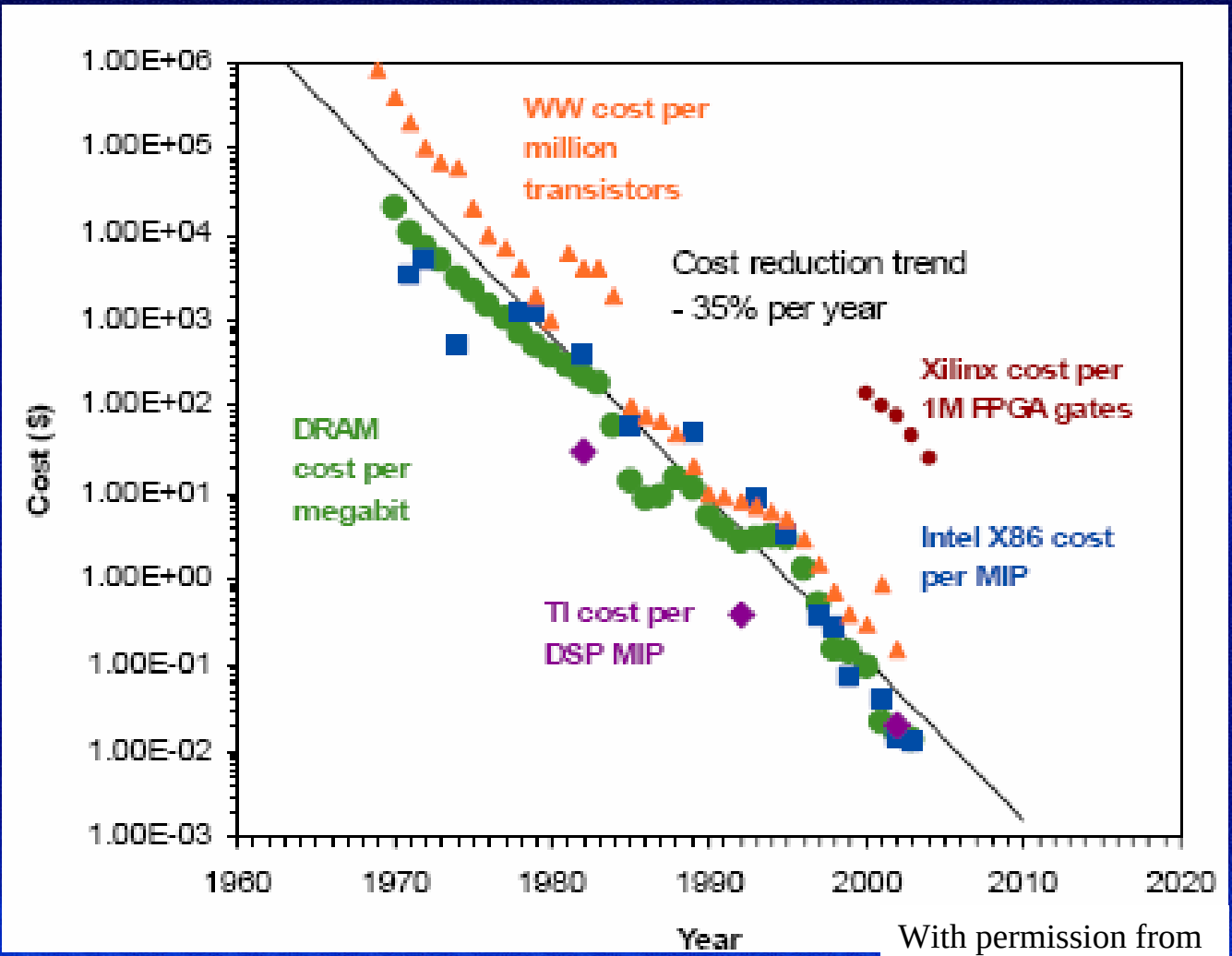
Exponential Cost Reduction

Cost per Transistor



Exponential Cost Reduction

Value to End User



With permission from IC Knowledge LLC

Technology Job 1

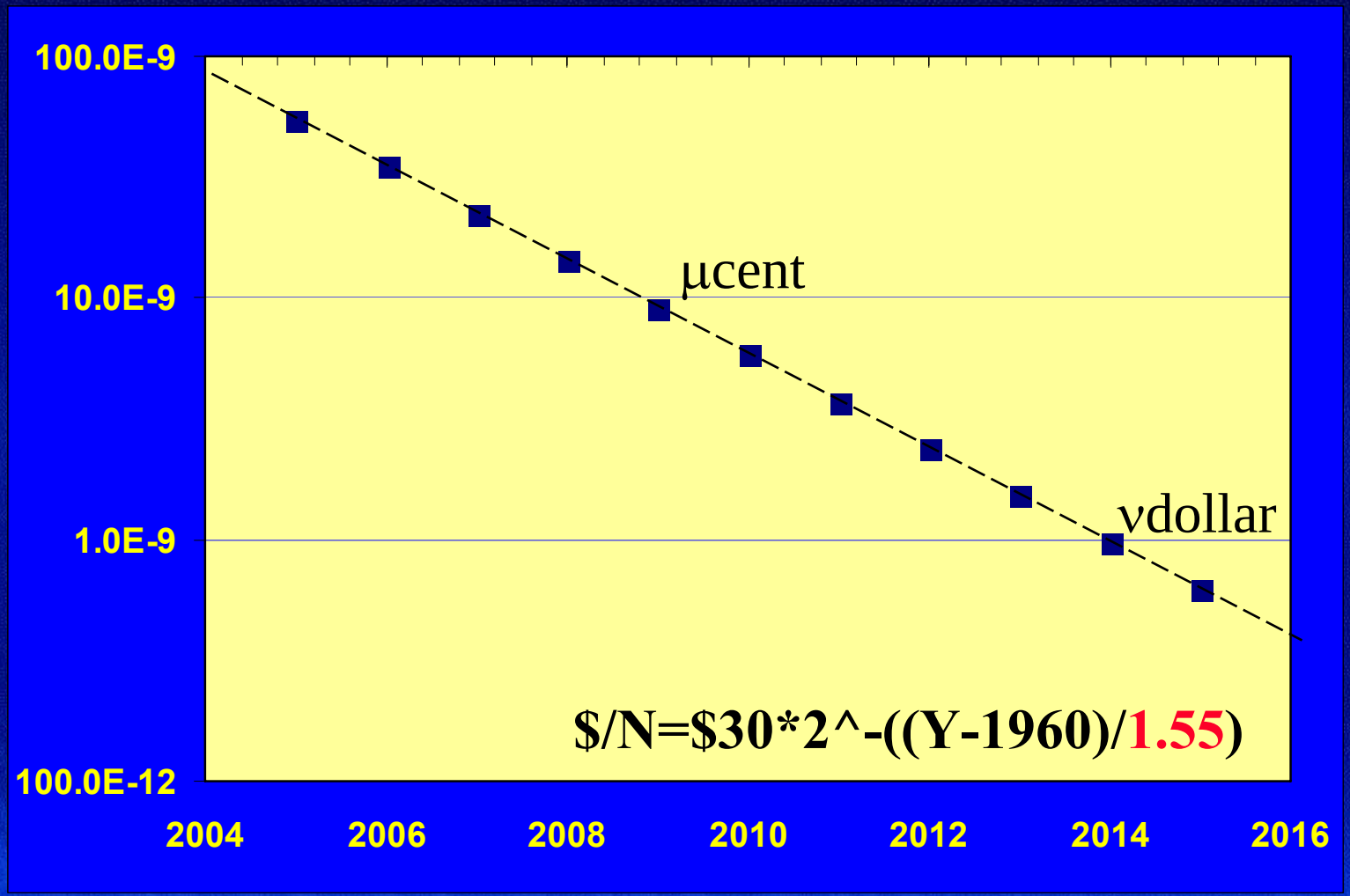
Promise of sustained reduction of information processing cost gave birth to IC industry.

Successful realization of this promise sustained semiconductor industry growth for 45 years.

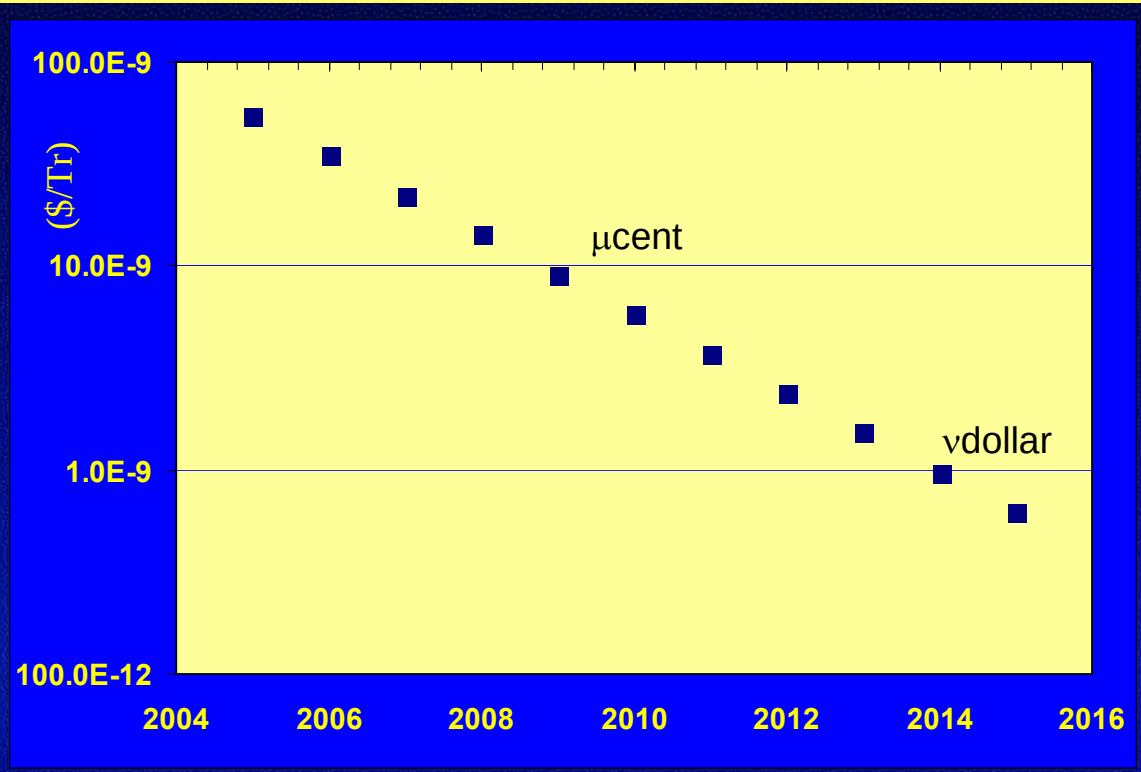
To extend happy and productive industry life Technology must continue to identify solutions that maintain exponential reduction in information processing cost at lowest research, development and manufacturing expense.

Our Job for Next 10 Years

Cost per Transistor -



Our Job for Next 10 Years



Scaling …… Solution that delivers:

Density Reduction ≥ 2x/Gen
World Class Yield
Wafer Cost Increase ≤ 1.10/Gen
R&D Cost Containment

Scaling – Intel 45 nm SRAM

(from 1/25/2006 M.Bohr announcement)

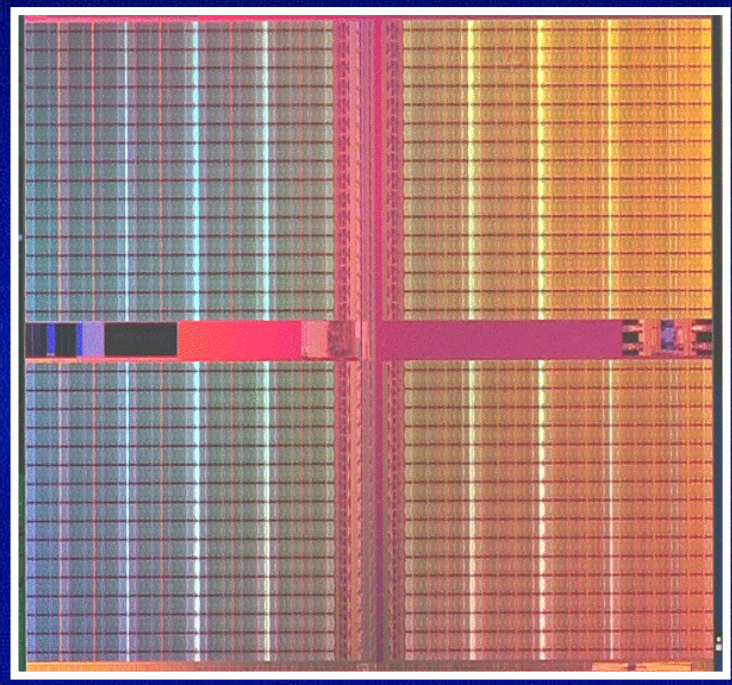
0.346 μm^2 cell

153 Mbit density

119 mm^2 chip size

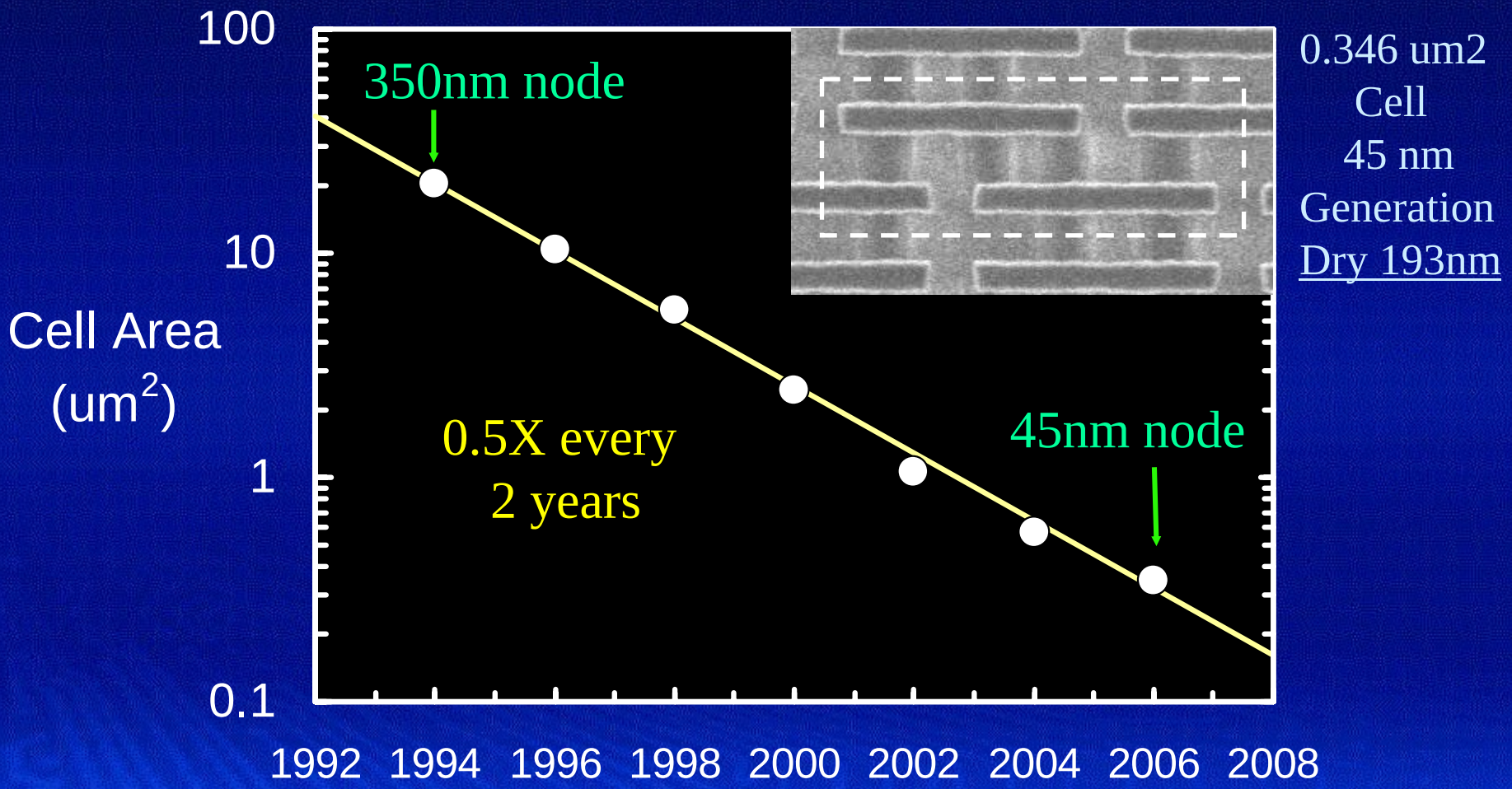
>1 billion transistors

Functional silicon in Jan '06

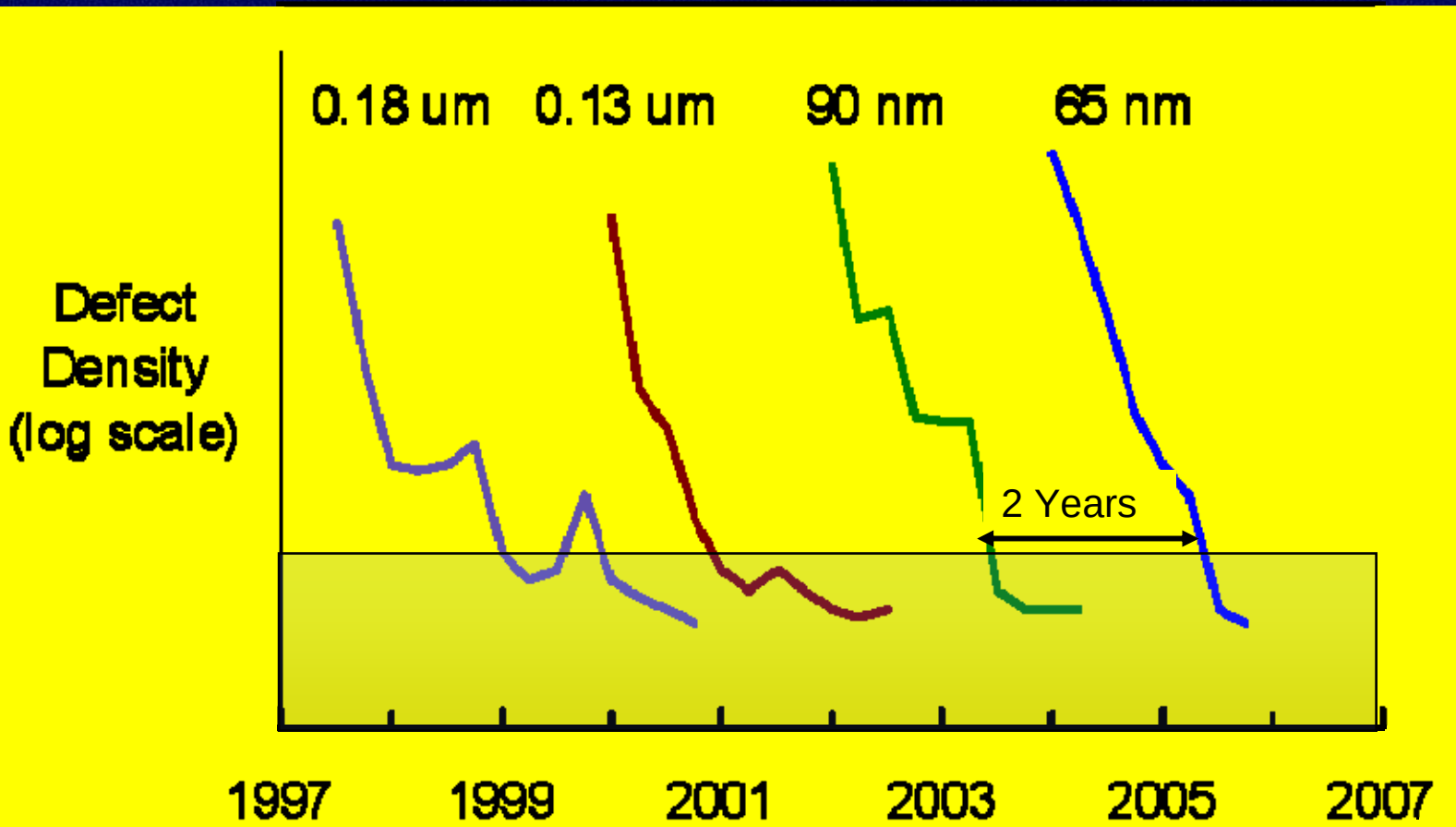


45 nm SRAM test vehicle includes all transistor and interconnect features to be used on 45 nm microprocessors

Intel's Density Scaling



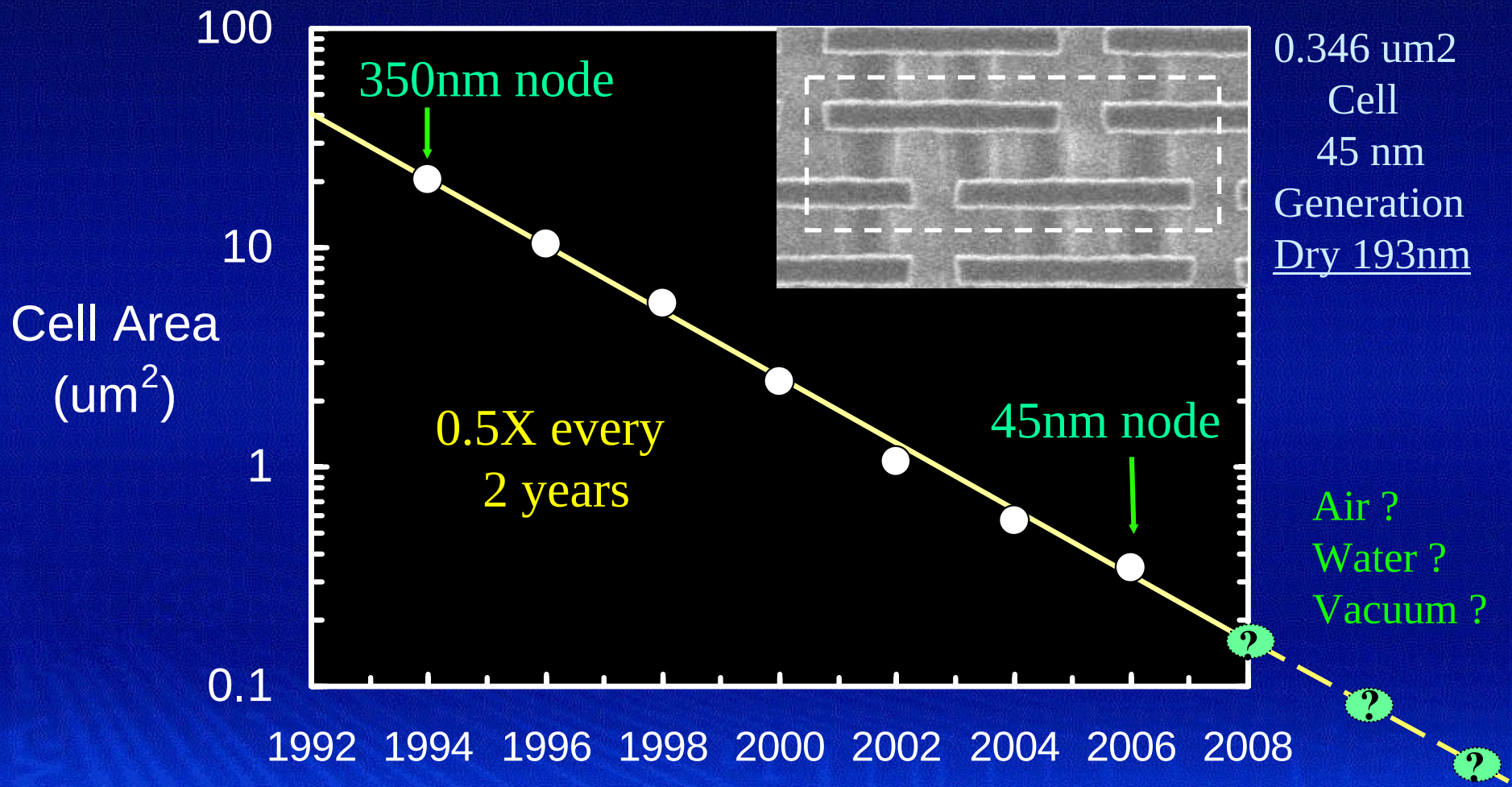
Predictable World-Class Yield on 2 Year Cycles



Copy Exactly! transfer methodology enables matched yield at new factory startup

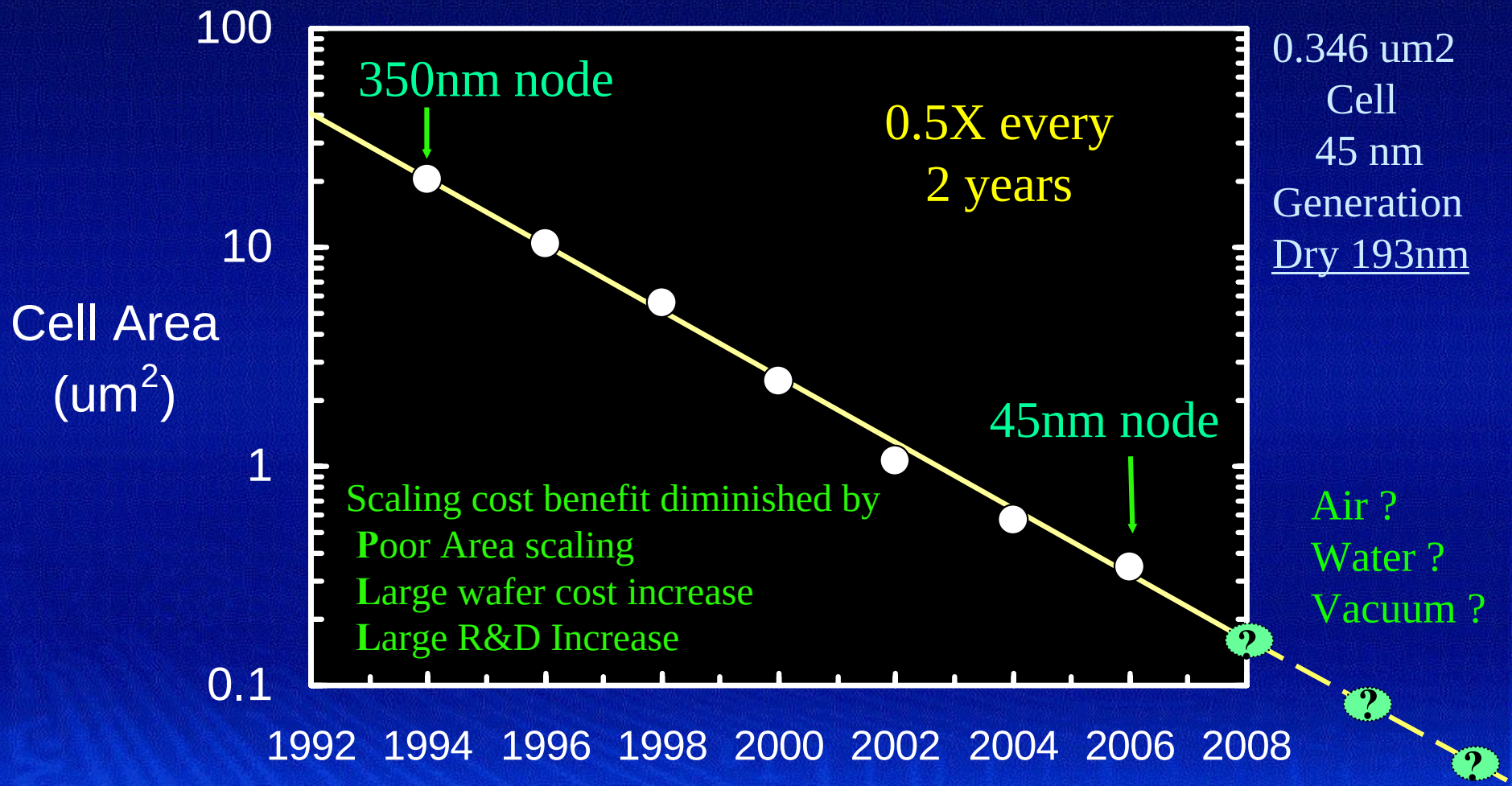
Area Density Scaling

Future SRAMs - Should we hold our breath?



Area Density Scaling

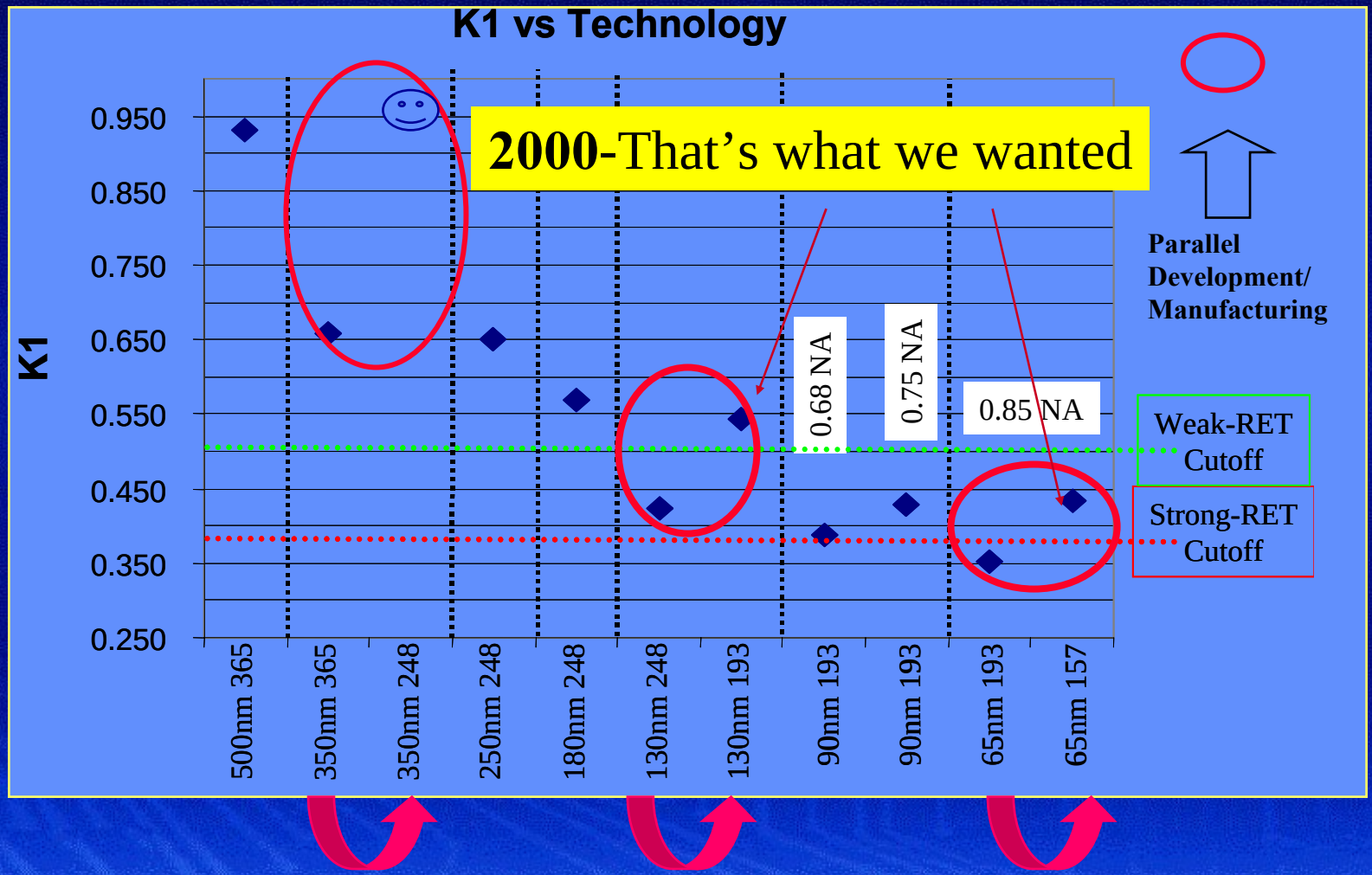
Yes, and avoid **PLL**!



“When you come to the fork in the road – take it”

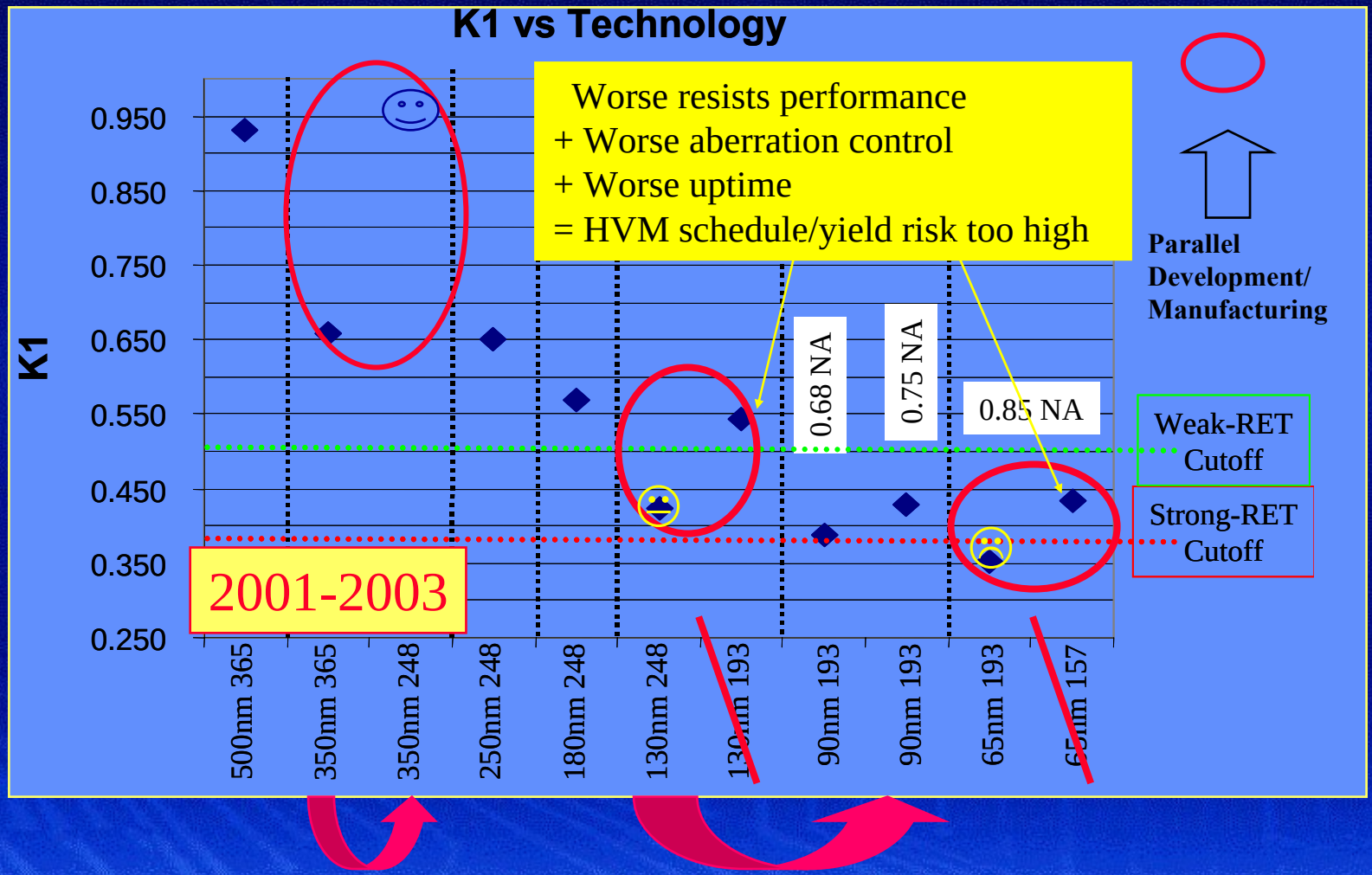
Yogi Berra

Scaling: Intel’s Dual Wavelength Strategy



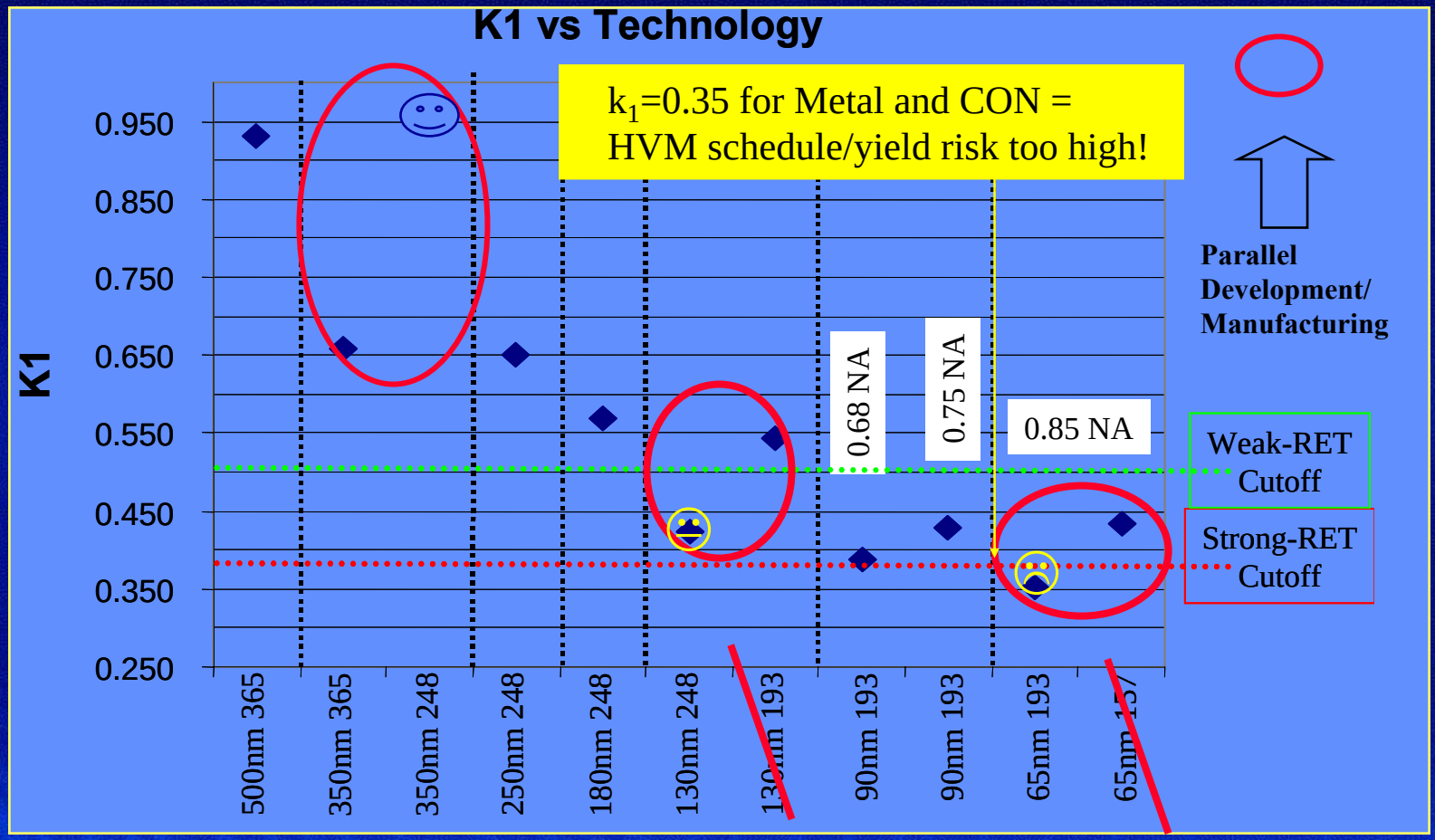
Intel's Dual Wavelength Strategy

That's what we got



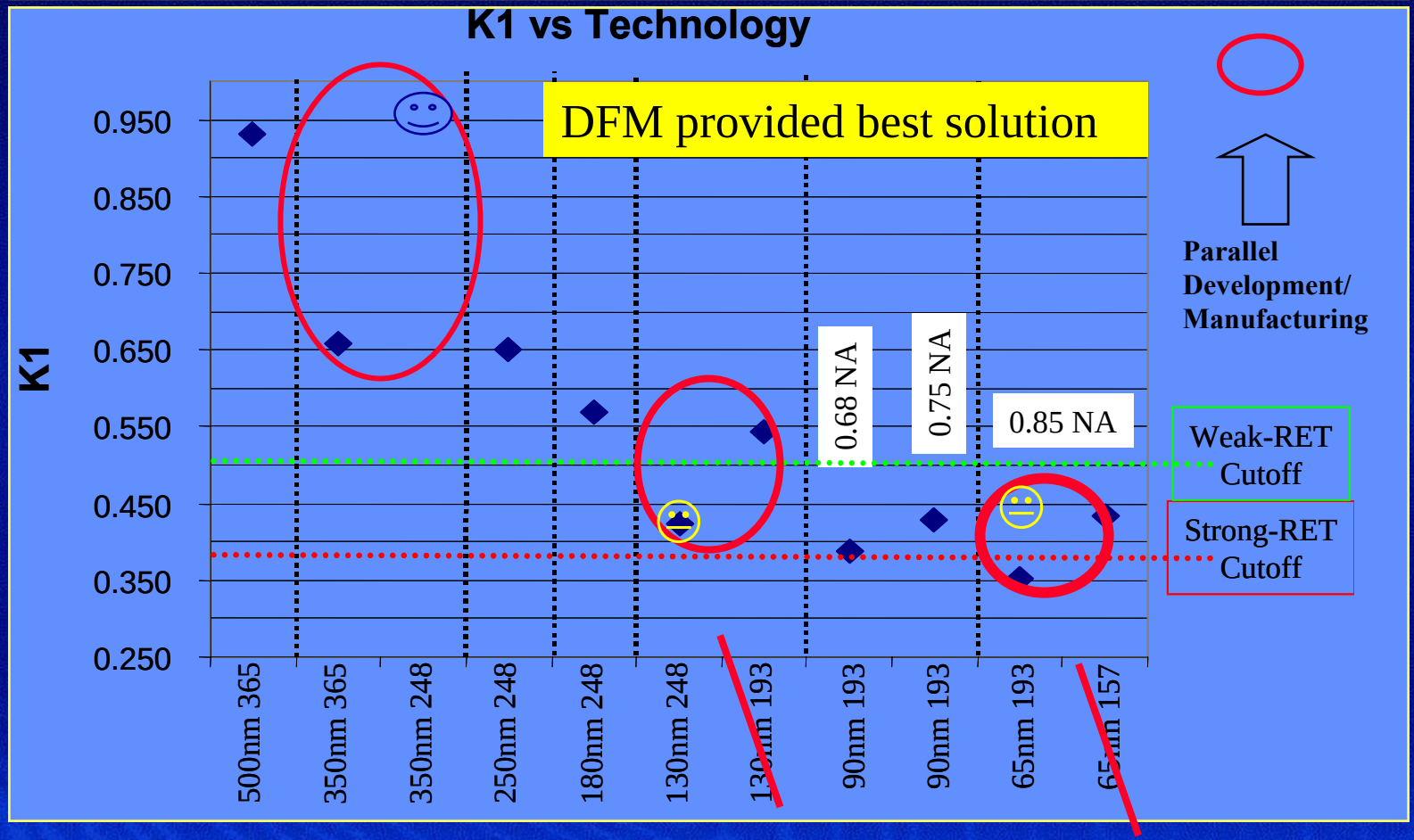
Intel's Dual Wavelength Strategy

Innovative solution required for 65nm node



Intel's Dual Wavelength Strategy

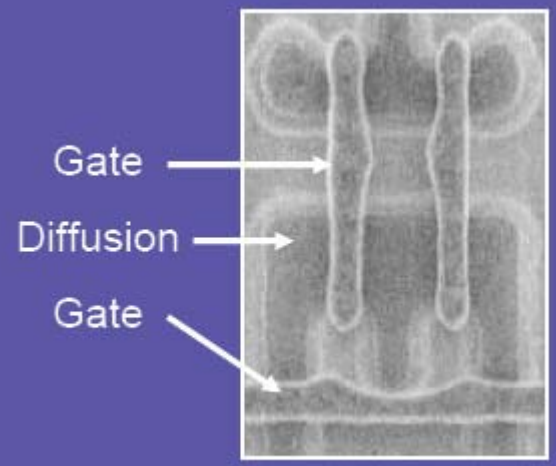
Architectural Innovation (developed in parallel) enabled Lithography solution acceptable for 65nm node High Volume Production



Necessity is mother of invention

65nm node 6T SRAM

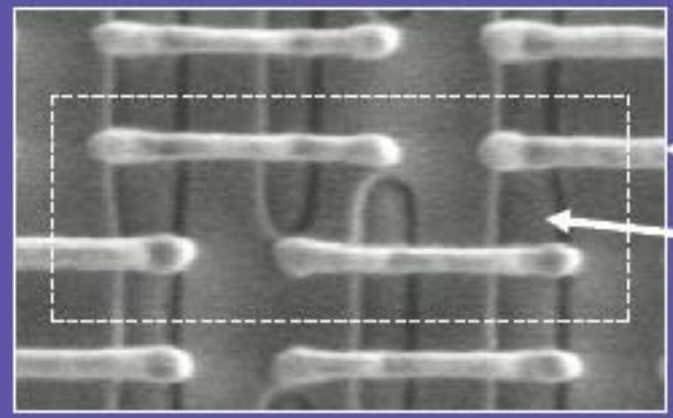
0.5X area reduction with 0.95x MT1 scaling



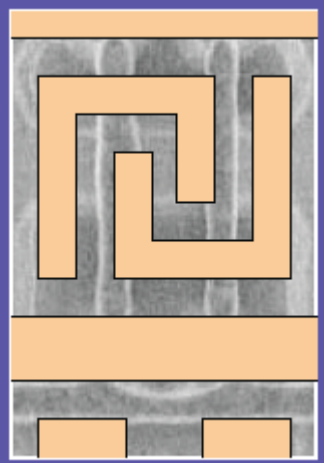
Traditional

65nm node
0.57um2

Cell

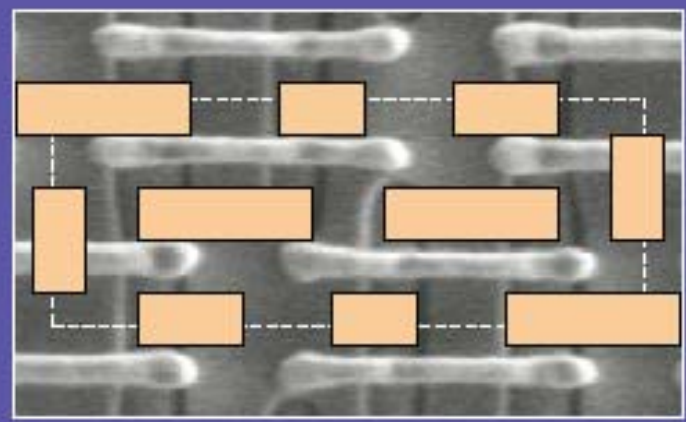


New



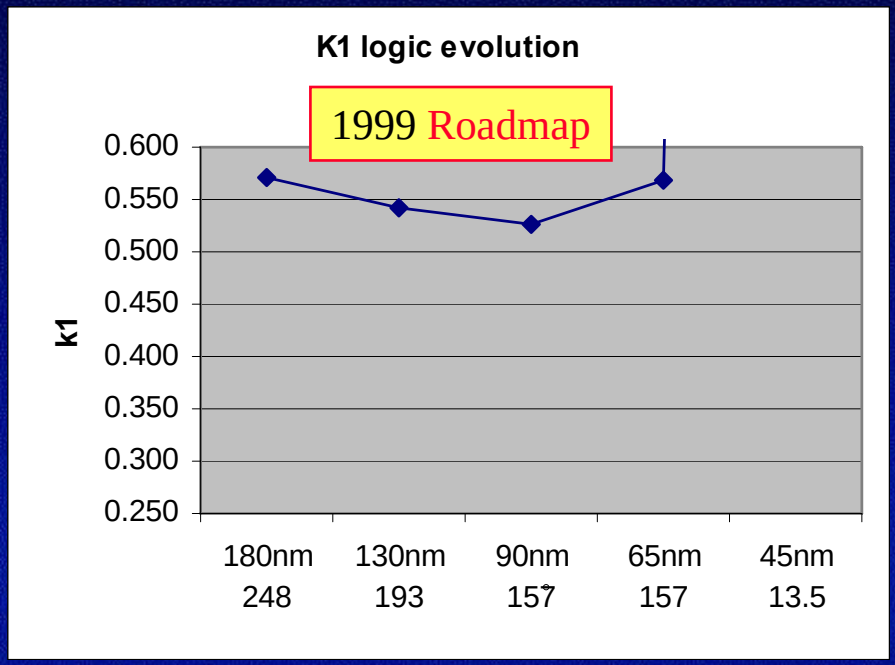
160nm

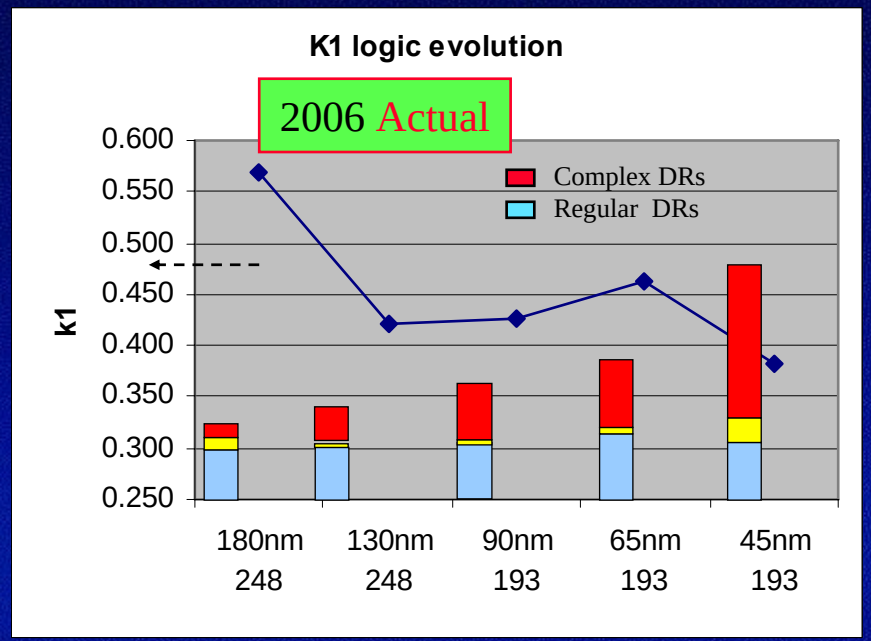
MT 1
Pitch



210nm

But…

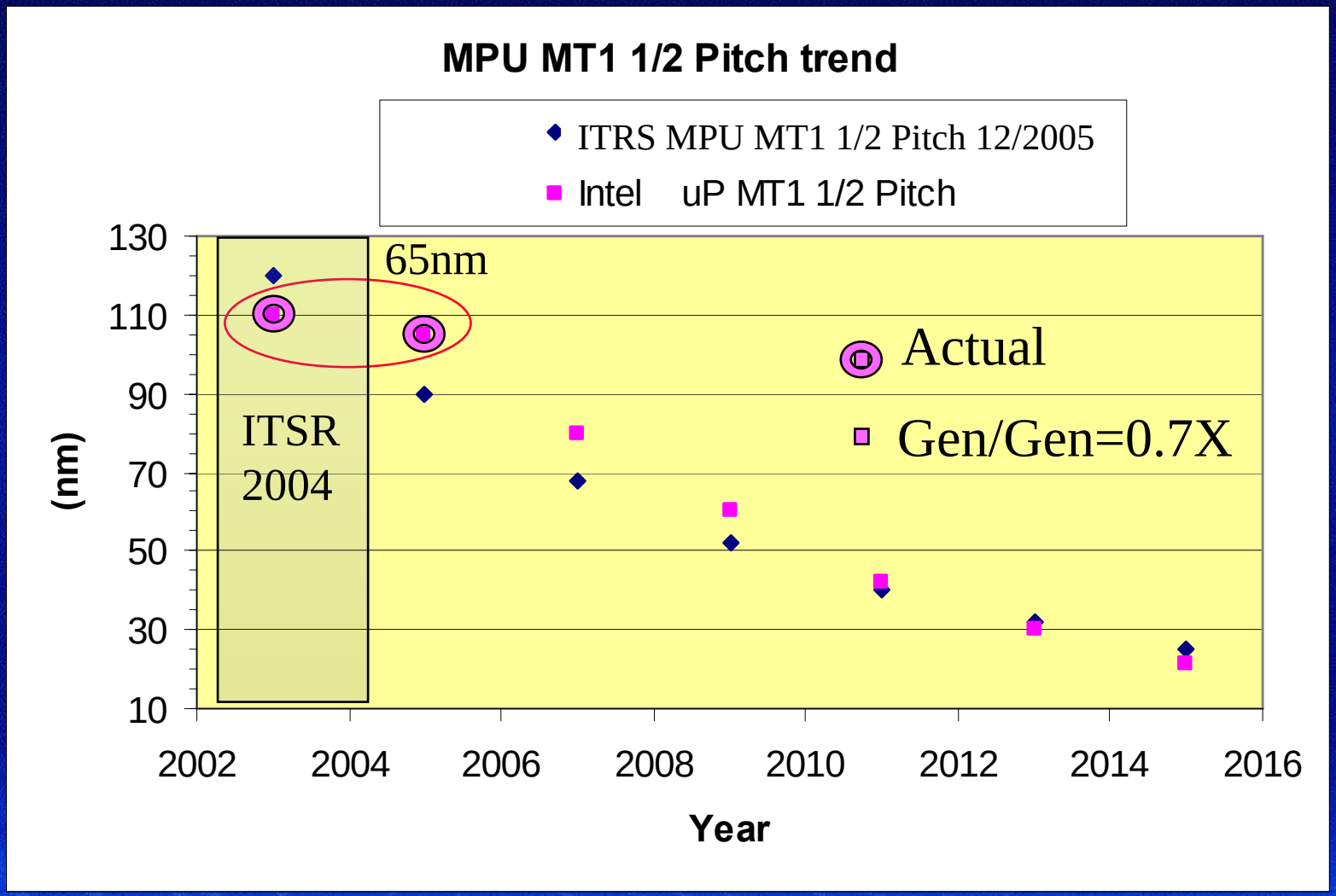




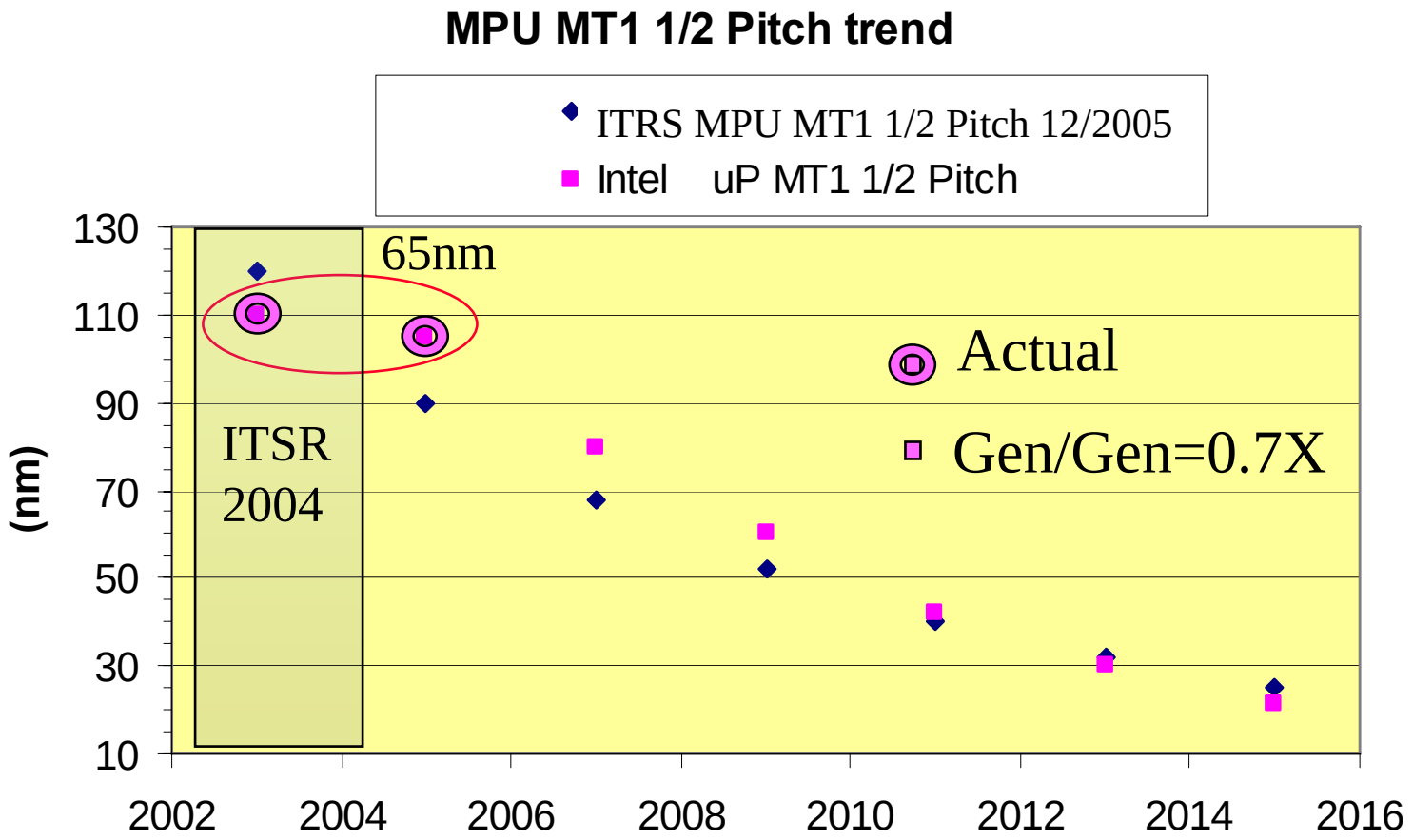
Late availability of 193nm technology, materials concerns with 157nm Litho, numerous issues with 13.4nm forced k1<0.45-0.40 on Logic.

Result: >10X increase in complex DRs, higher mask cost,
Same: 2 year Technology cycle, Fast Ramp, High yield!

New 6T SRAM
Impact on Lithography

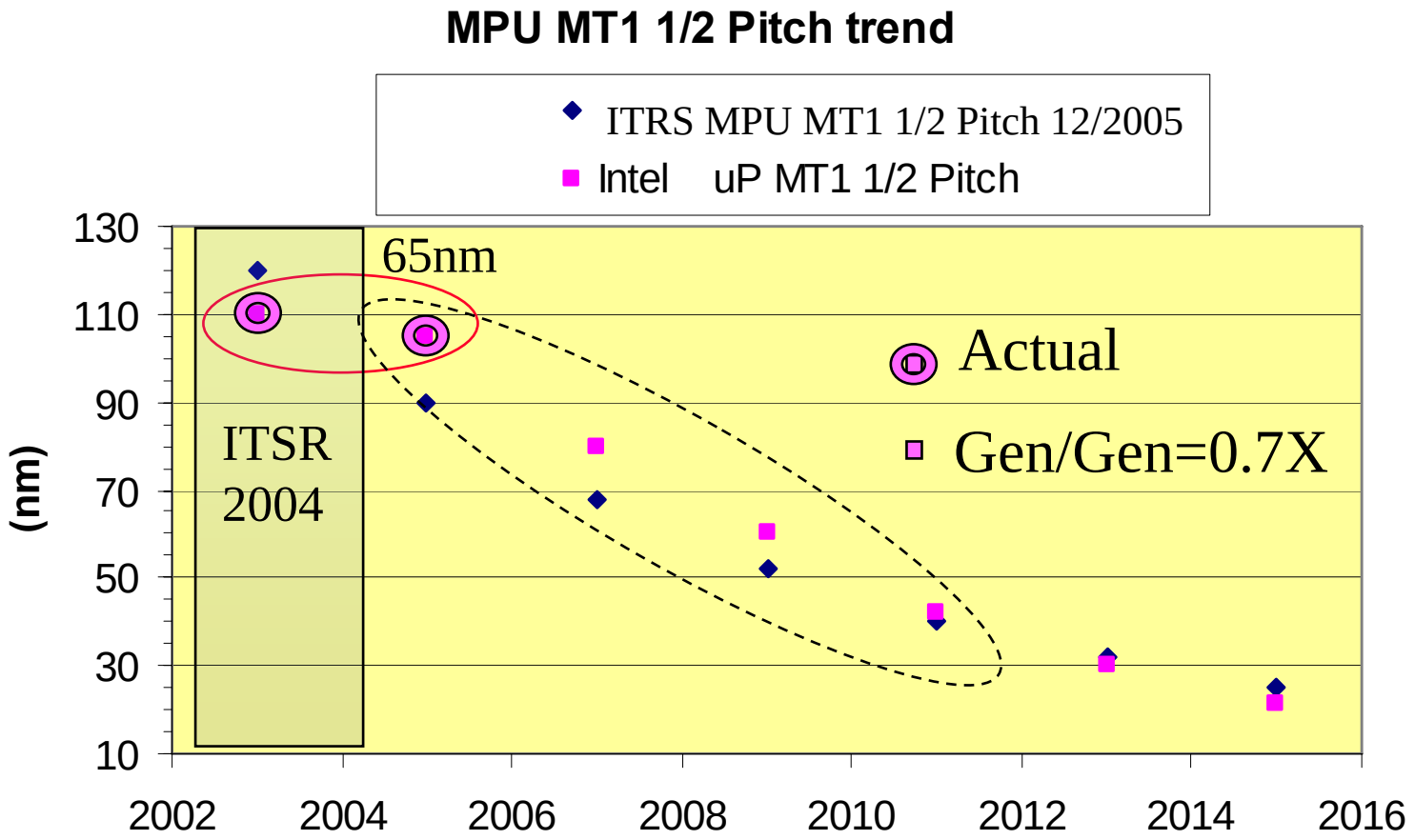


New 6T SRAM
Impact on Lithography



Fully Integrated Device Manufacturer structure allowed to continue 2X/Gen Density Scaling with available technology

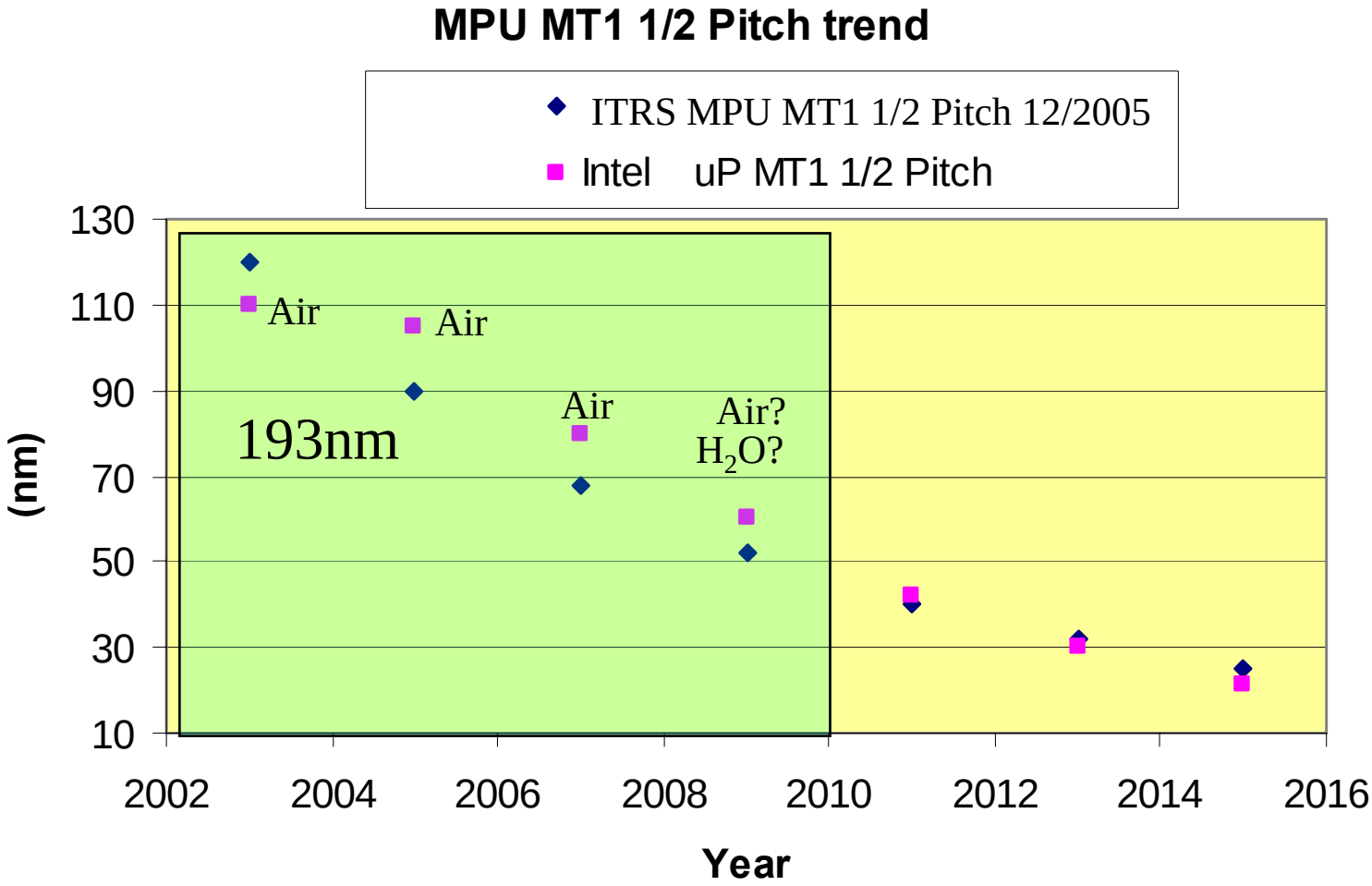
New 6T SRAM
Impact on Lithography



And brought additional benefits for 3 more generations

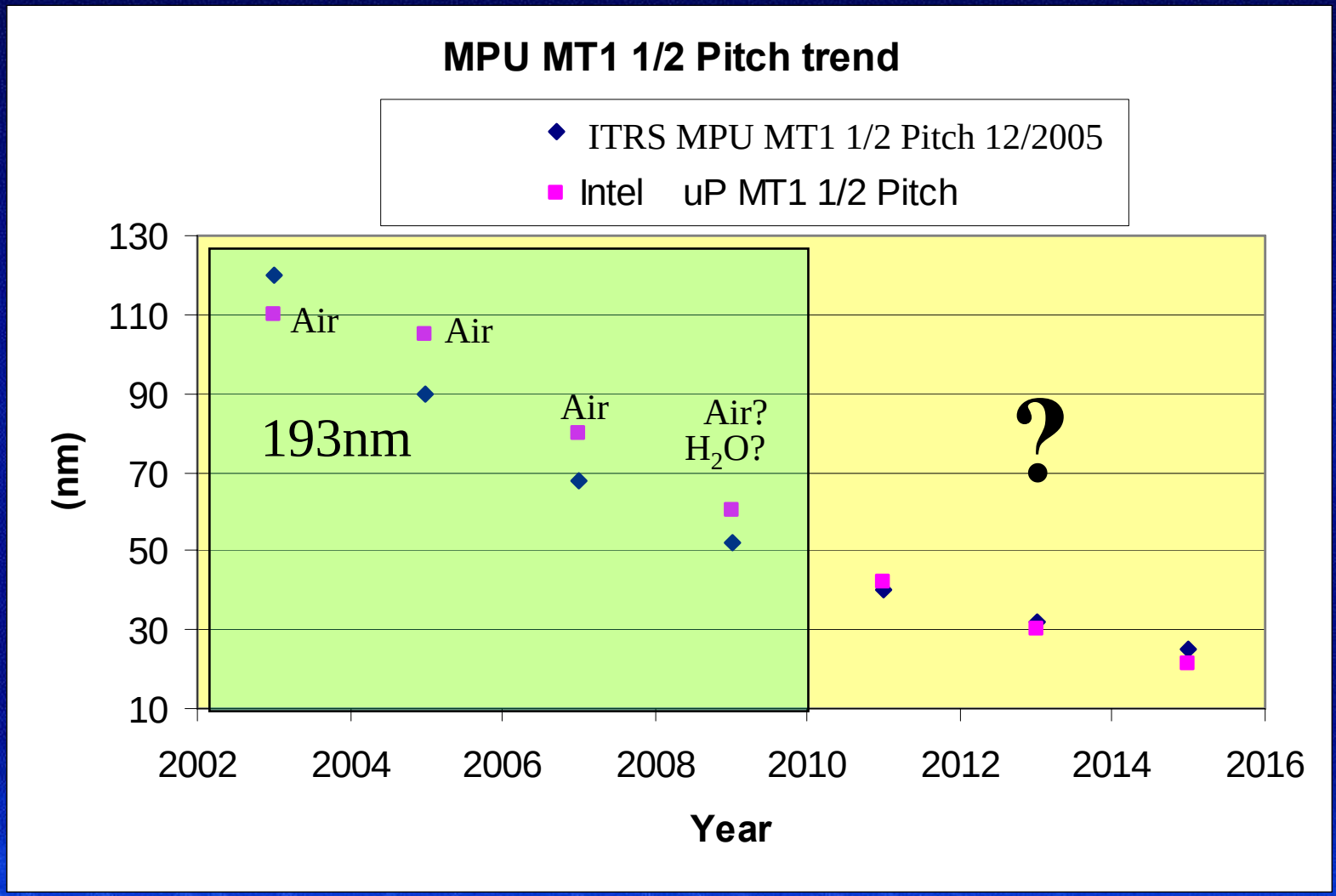
New 6T SRAM

ArF through Intel's 32nm node/2009 HVM



New 6T SRAM

ArF through Intel's 32nm node/2009 HVM



Moore's Law is there to set common Goals.

Power of Moore's Law observation and prediction was, is and will be for foreseeable future to provide common, easily understood quantified metric for everyone in semiconductor and IT economy to synchronize their efforts toward historically based, well defined, sustainable and mutually rewarding growth goals in the future.

Moore's Law is there to set common Goals.

Power of Moore's Law observation and prediction was, is and will be for foreseeable future to provide common, easily understood quantified metric for everyone in semiconductor and IT economy to synchronize their efforts toward historically based, well defined, sustainable and mutually rewarding growth goals in the future.

Roadmaps are there to debate the Path.

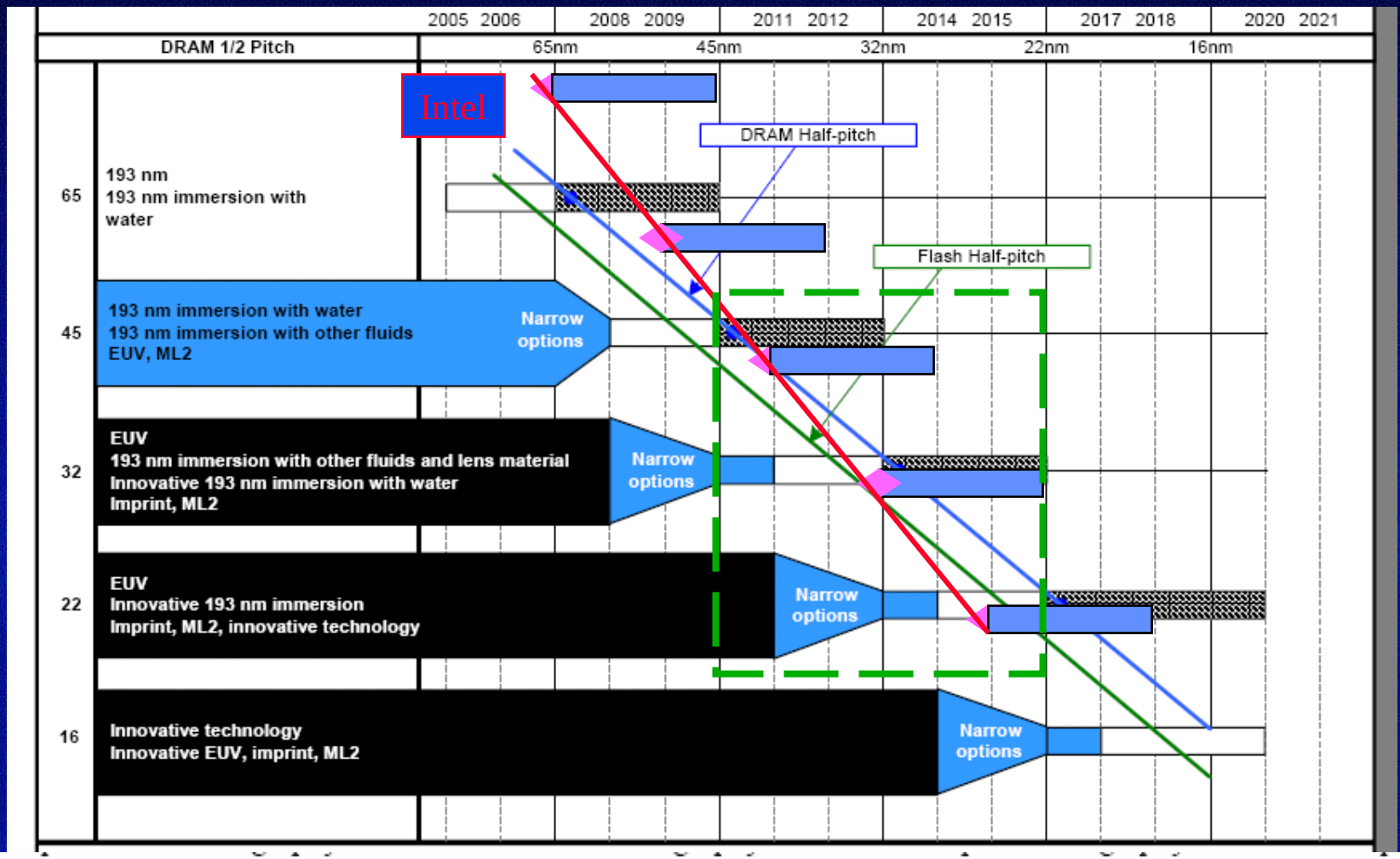
Moore's Law is there to set common Goals.

Power of Moore's Law observation and prediction was, is and will be for foreseeable future to provide common, easily understood quantified metric for everyone in semiconductor and IT economy to synchronize their efforts toward historically based, well defined, sustainable and mutually rewarding growth goals in the future.

Roadmaps are there to debate the Path.

Path to achieving those goals (Roadmap) was, is and will be subject to unending debates as it reflects fundamental uncertainty of assessing risks to schedule and yields of ever more complex novel technologies over extending existing "tried and true" approaches beyond its originally defined limits in the absence of data.

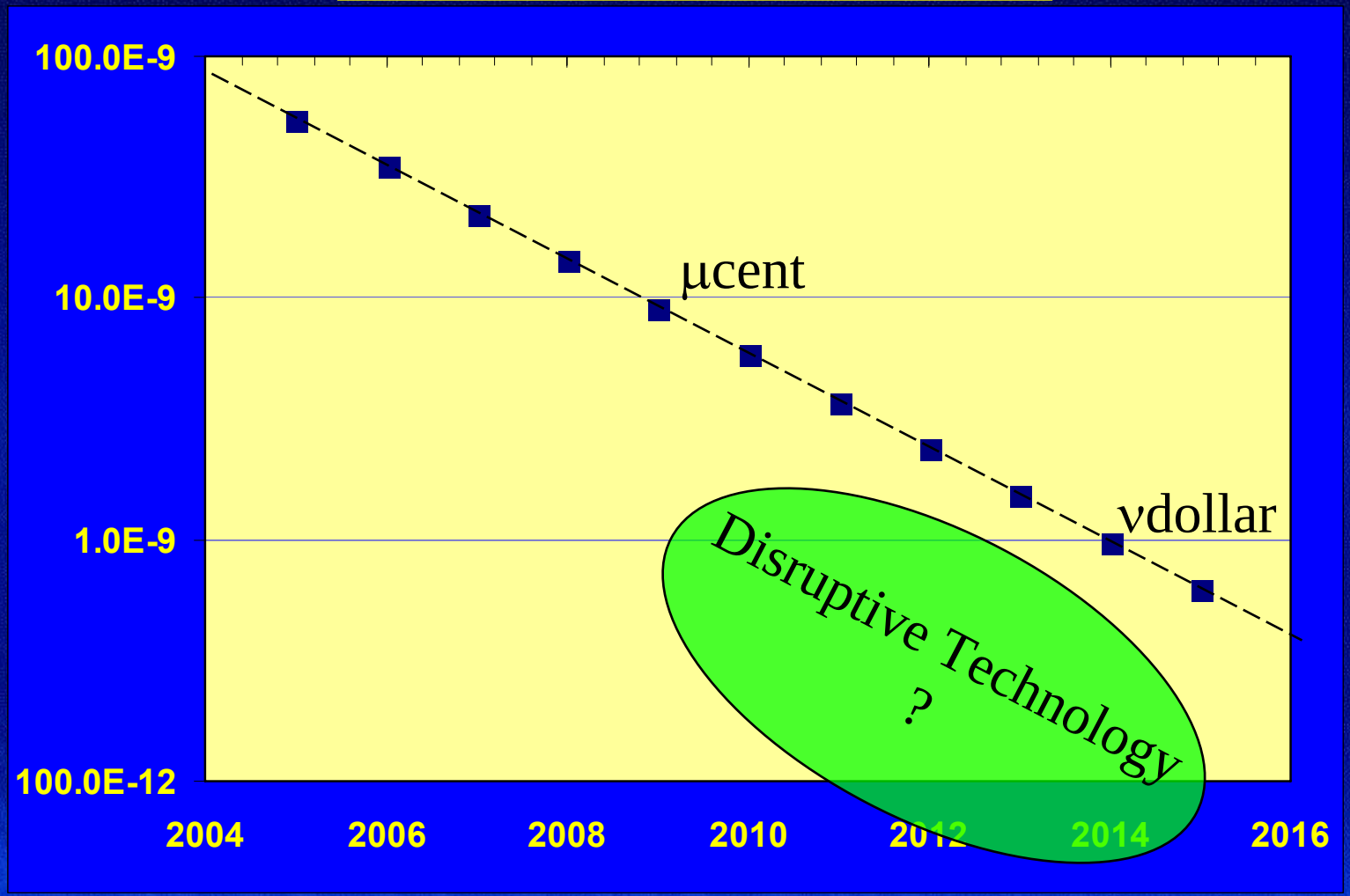
ITRS 2005 (Dec. 2005)



lens materials with high index and higher index fluids can be developed in time. Research is also ongoing into breaking the pattern into two masks, each mask having minimum half pitch two times the minimum half pitch to be printed on the wafer. This dual-mask exposure technique could be used to extend 193 nm immersion lithography beyond DRAM 32 nm half pitch if resists suitable for double exposure and adequate mask alignment could be developed. Software for optimally dividing the pattern into two masks would need to be developed, and the use of two masks would have to be less expensive than alternative technologies.

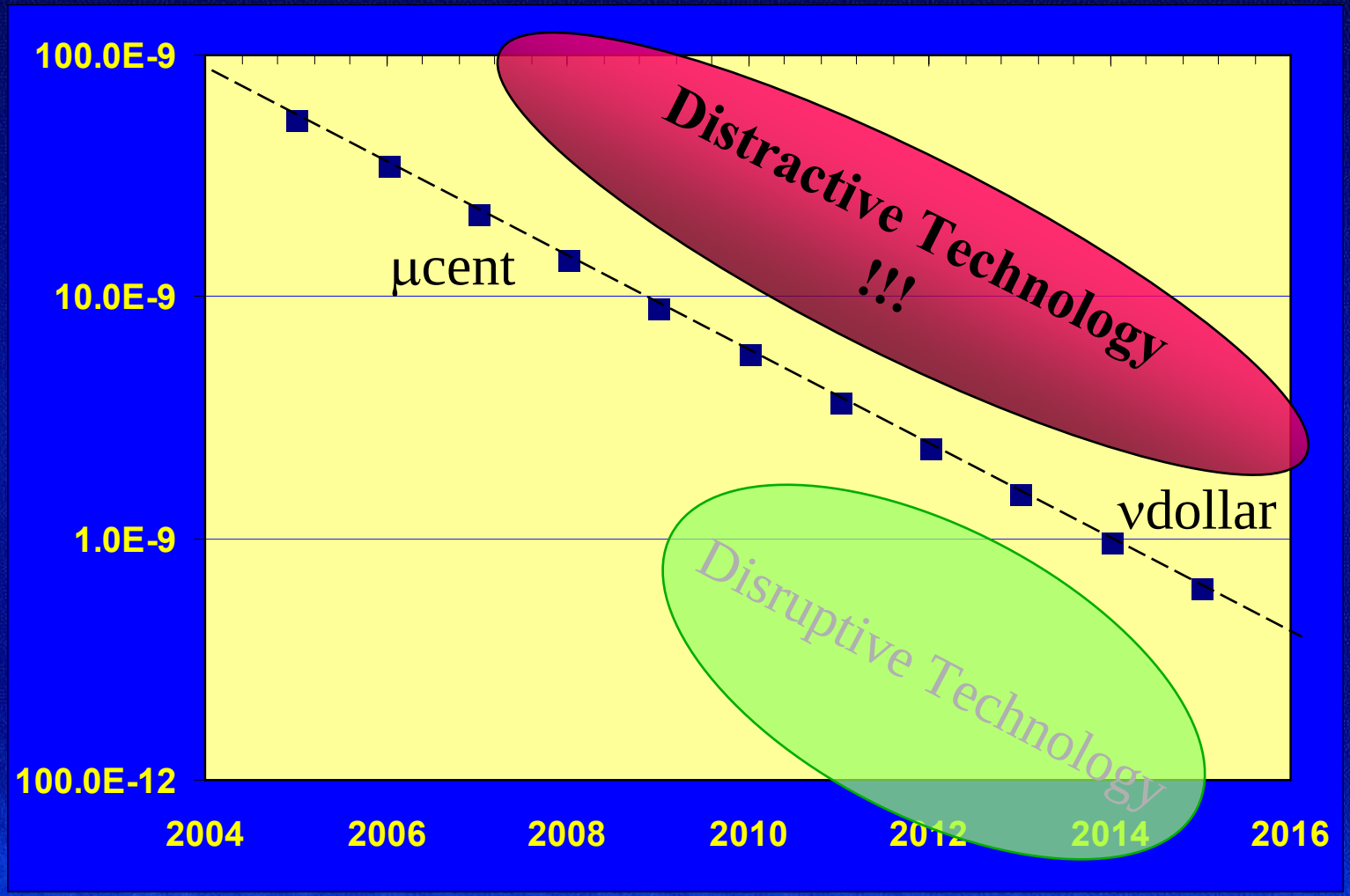
Disruptive – Has to be better!

$/N<$30*2^-((Y-1960)/1.55)



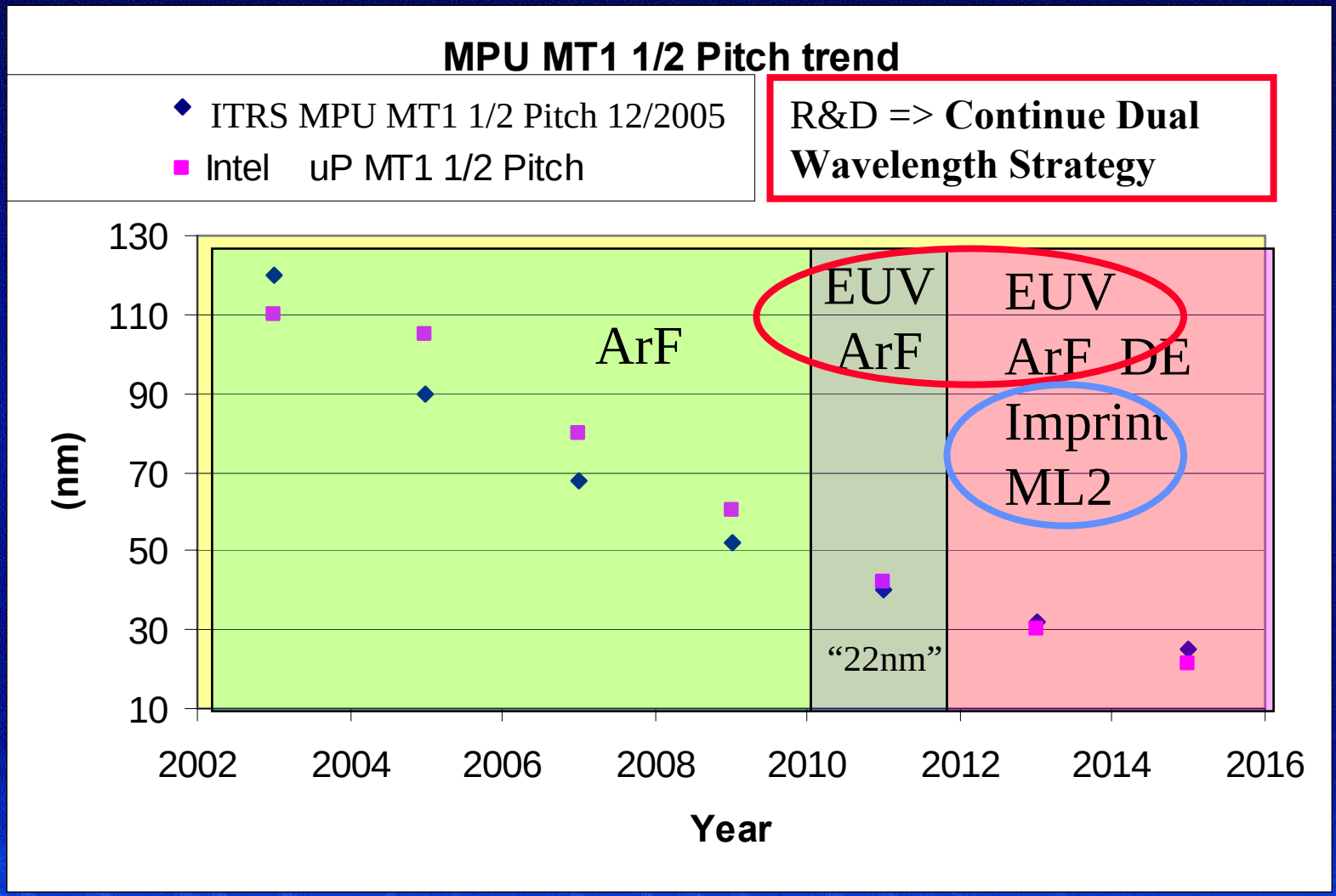
Distractive Technology

$/N>$30*2^-((Y-1960)/1.55)



Multiple Options for 2011 – 2015

Continue Dual Wavelength R&D Strategy



Next 10 Years - Dual λ Options

Multiple Patterning Options with Existing Materials

HVM Year/Tool	**k1** SE	Litho Challenge from Previous Generation	Availability Proof by
2007 193/0.93	**0.38**	**Evolutionary**	**Done**
2009 193/0.93	**0.29**	**New, RET**	**2006**
193/1.20	**0.37**	**New, Defects, dry/wet OL**	**2006**
2011 193/0.93DE	**0.40**	**New, SE/DE methodology, CD/OL**	**2008**
193/1.35	**0.29**	**Evolutionary if 193/1.2 in 2009**	**2008**
13.5/0.25	**0.78**	**New, Defects, TPT/LER; EUV/193 OL**	**2009**
2013 193/0.93DE	**0.29**	**Evolutionary if 0.93DE in 2011**	**2008**
193/1.20DE	**0.37**	**Evolution if 193i,DE in 2009,2011**	**2009**
13.5/0.35	**0.78**	**Evolutionary if EUV in 2011**	**2011**
2015 193/1.35DE	**0.29**	**Depends on 2009-2013 choice**	**2012**
13.5/0.35	**0.54**	**NA=0.35 might not be enough**	**2012**

Scaling – Next 10 Years

Key considerations

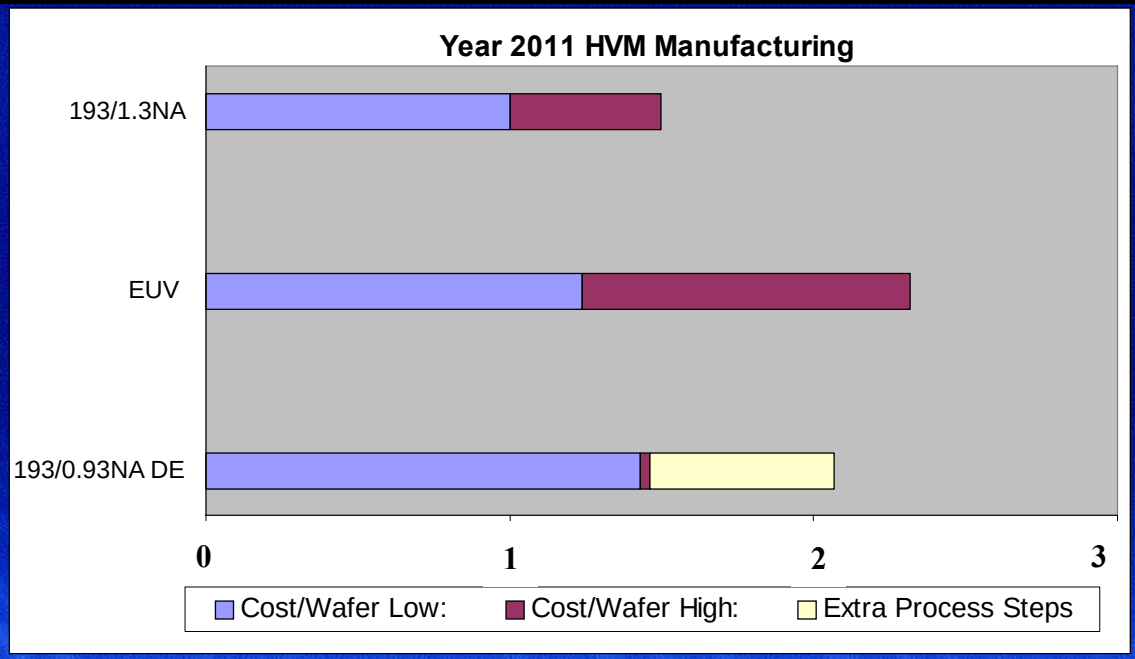
- **Proof of Availability needed for high yield HVM.**
- **Option that maximizes yield and minimize the cost will be chosen**
- **Final Lithography determination must be made no later then 1.5 years before HVM**
- **Development schedule will put strong pressure to down select winning technology 2-2.5 years prior to HVM Start.**

Each node selection guarantees interesting life for all of us!

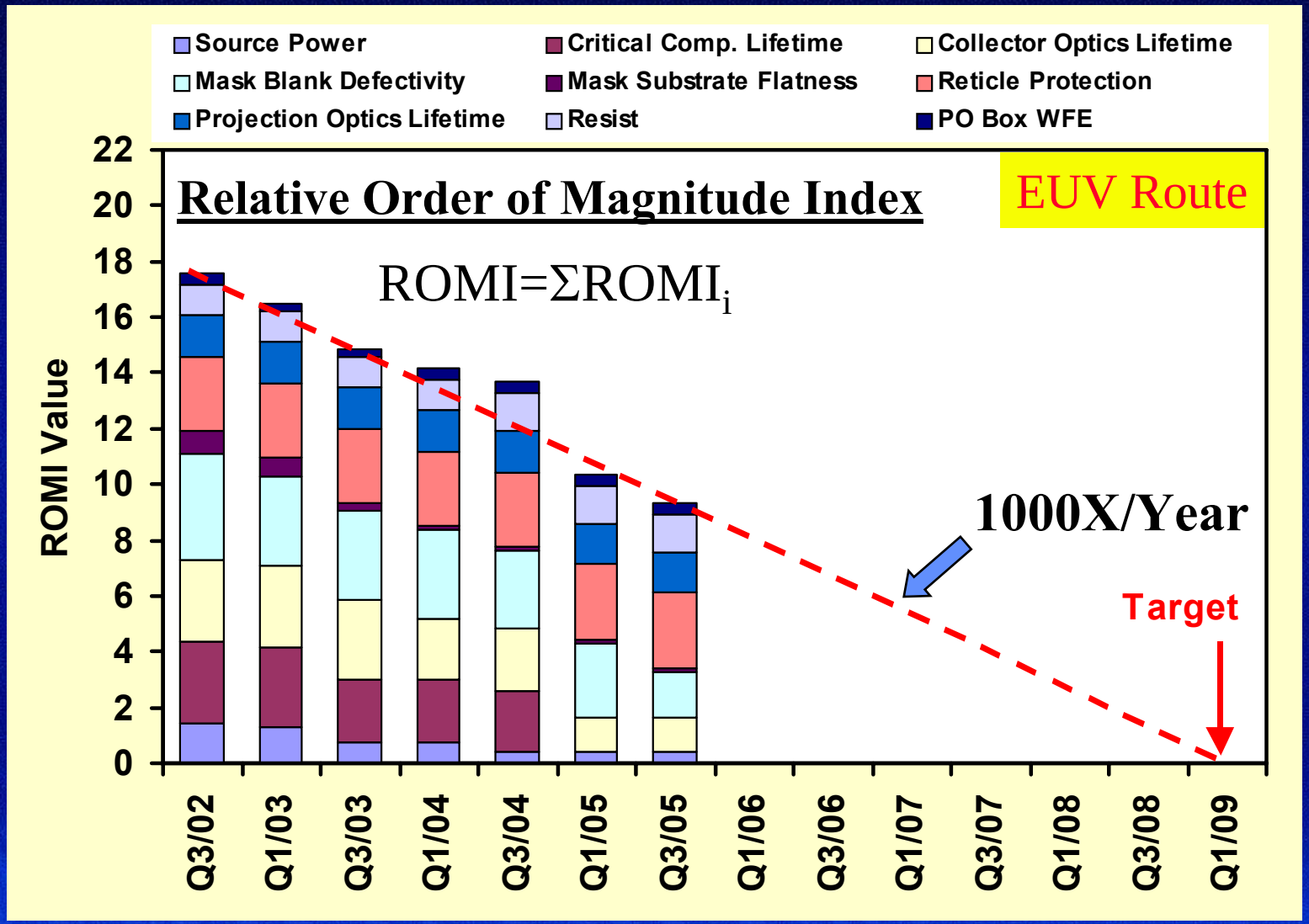
Next 10 Years - Dual λ Options

EUV promise better process margins, comparable COO

HVM Year/Tool		k1 SE	Litho Challenge from Previous Generation	Availability Proof by
2011	13.5/0.25	0.78	New, Defects, TPT/LER; EUV/193 OL	2010
2013	13.5/0.35	0.78	Evolutionary if EUV in 2011	2011
2015	13.5/0.35	0.54	NA=0.35 might not be enough	2012



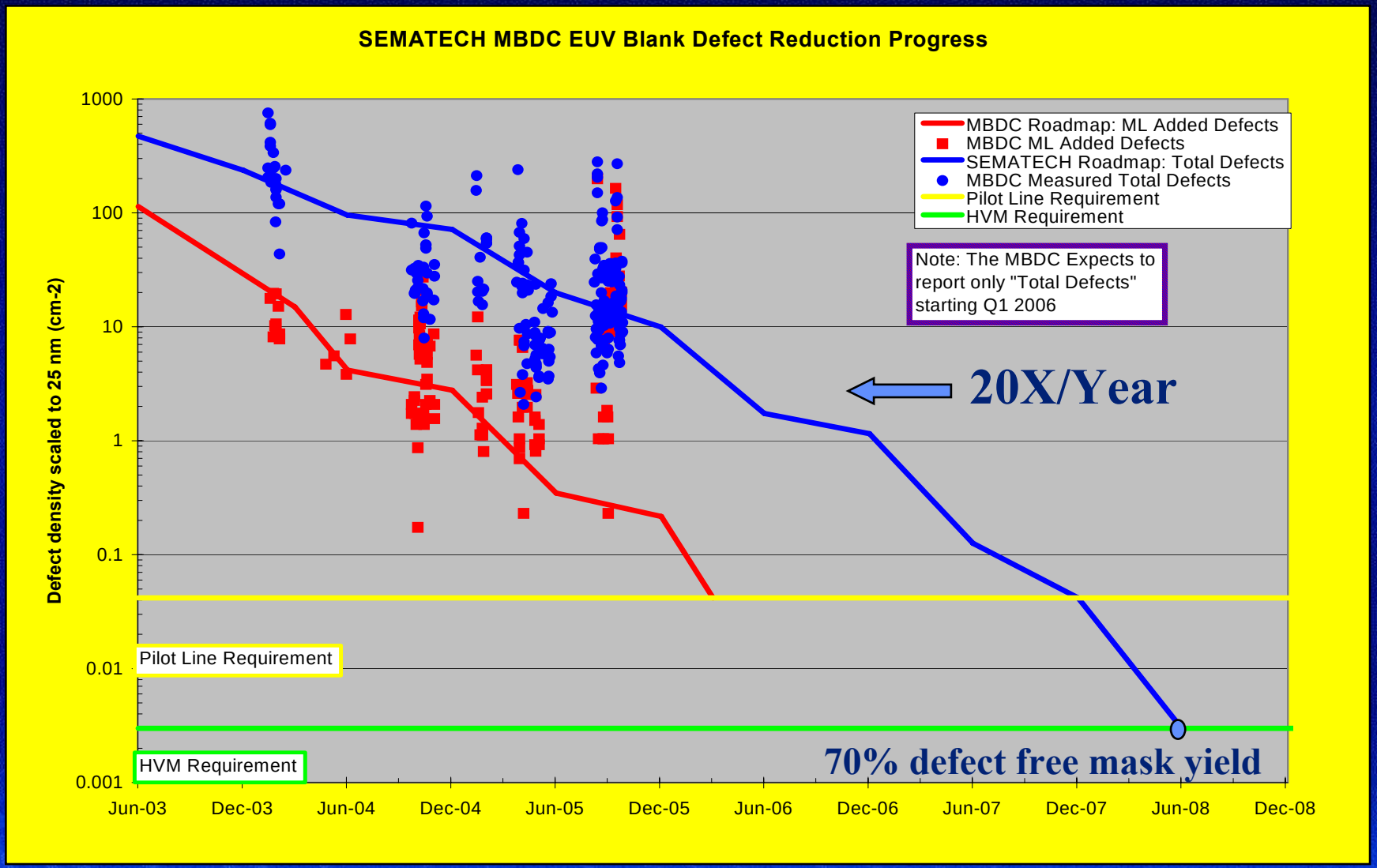
Next 10 Years - Dual λ Options



Source:ISMT

Next 10 Years - Dual λ Options

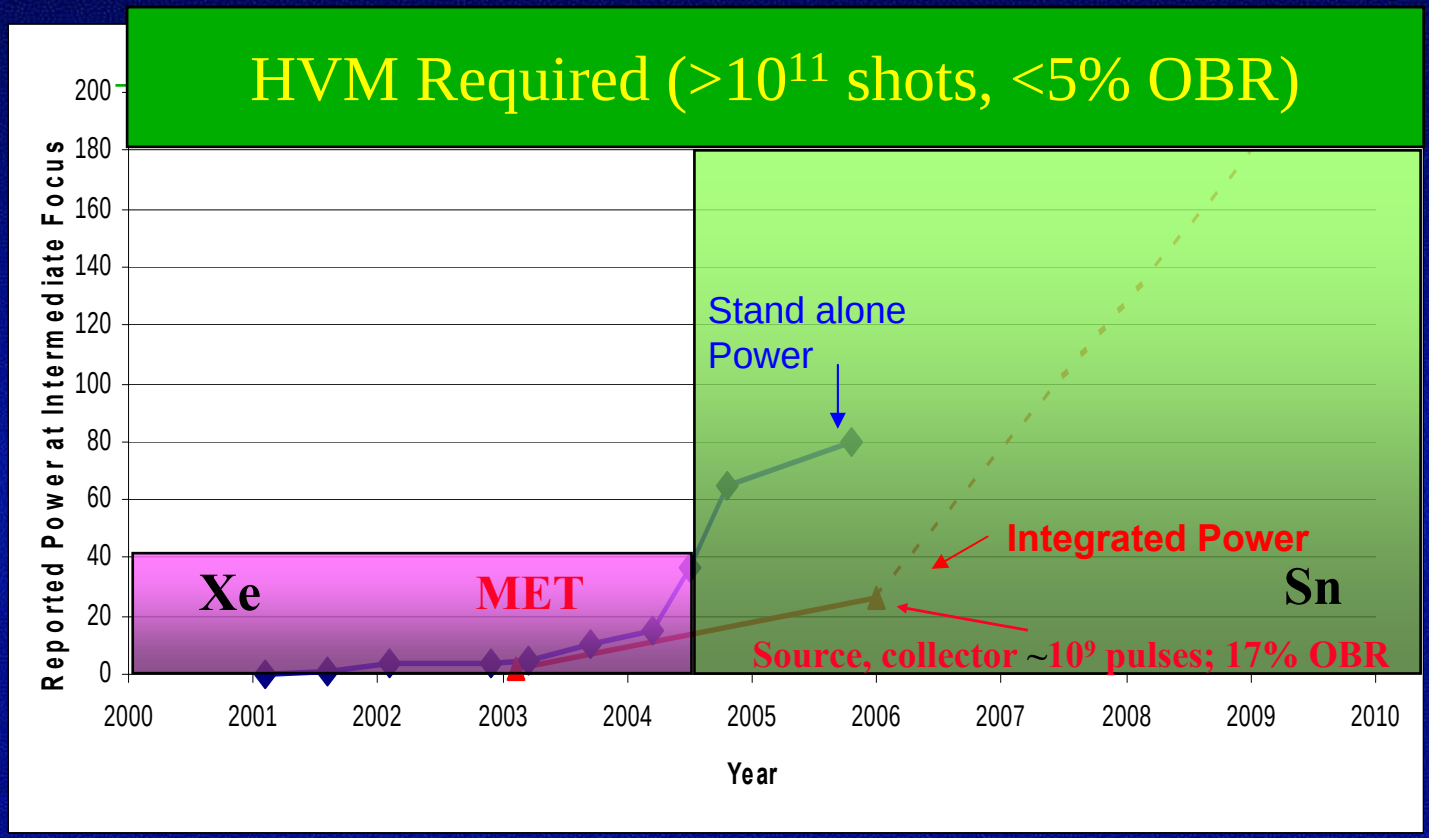
EUV Route – Mask Defects



Courtesy ISMT

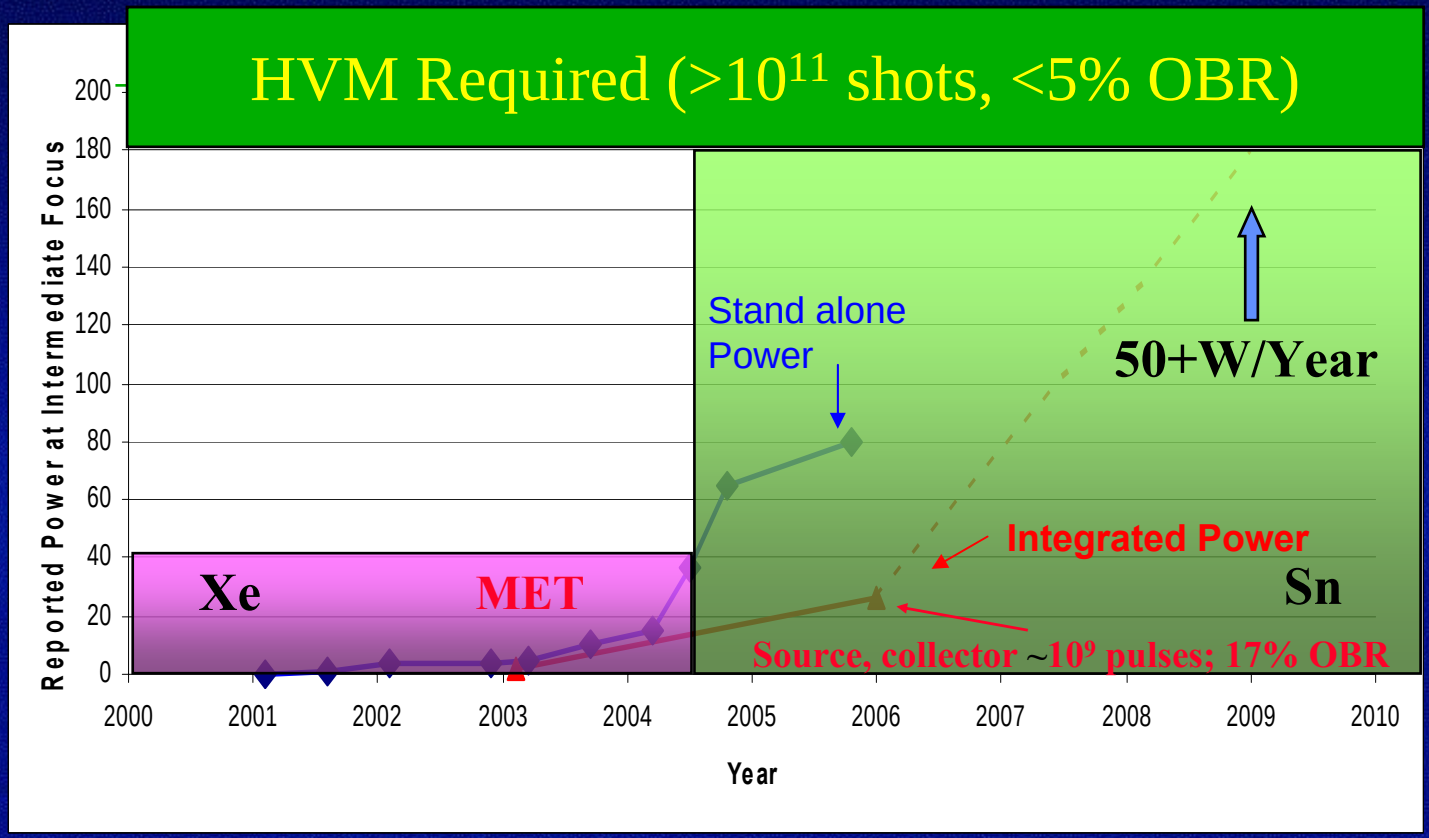
Next 10 Years - Dual λ Options

EUV Route – Source Power



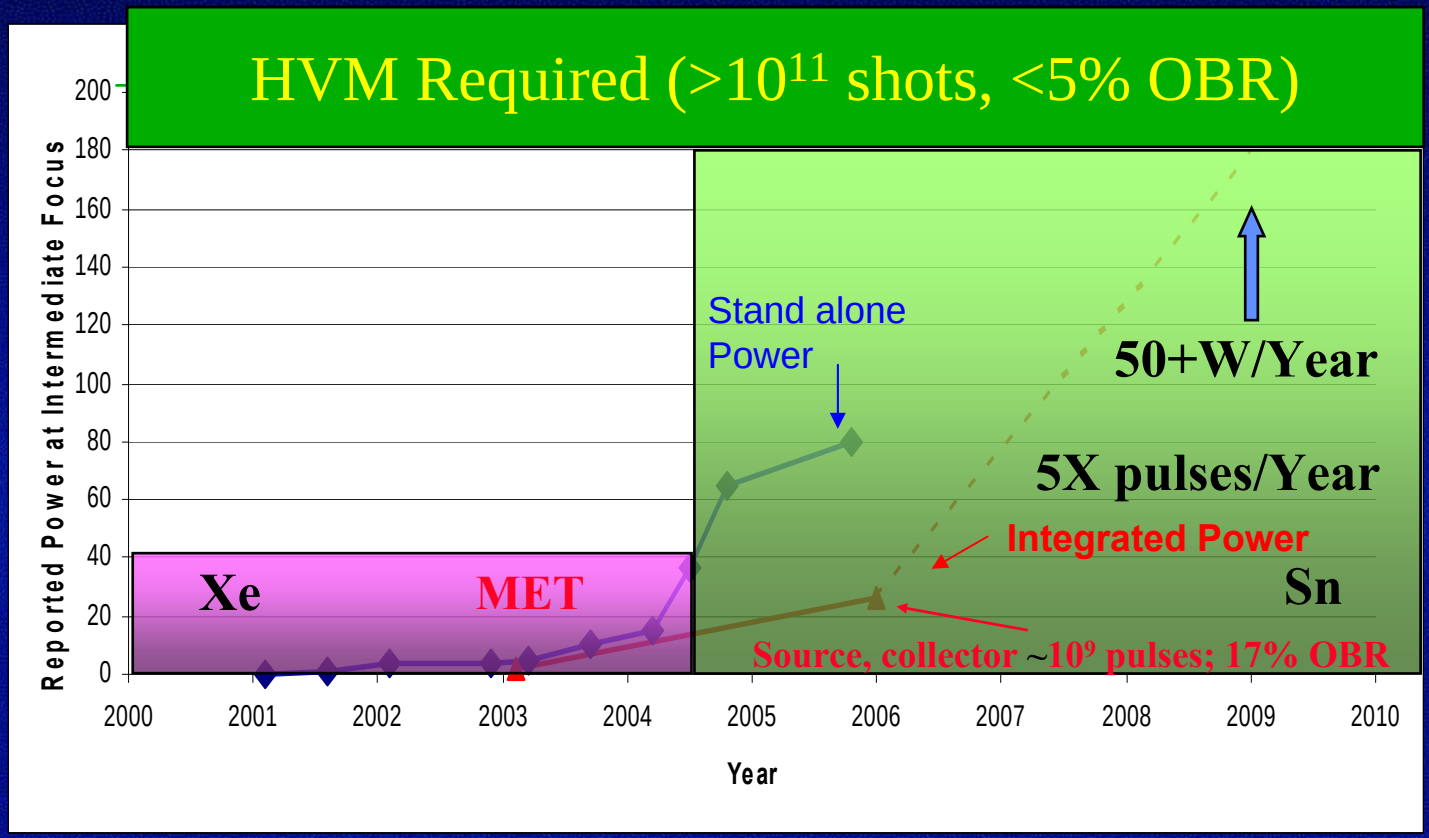
Next 10 Years - Dual λ Options

EUV Route – Source Power



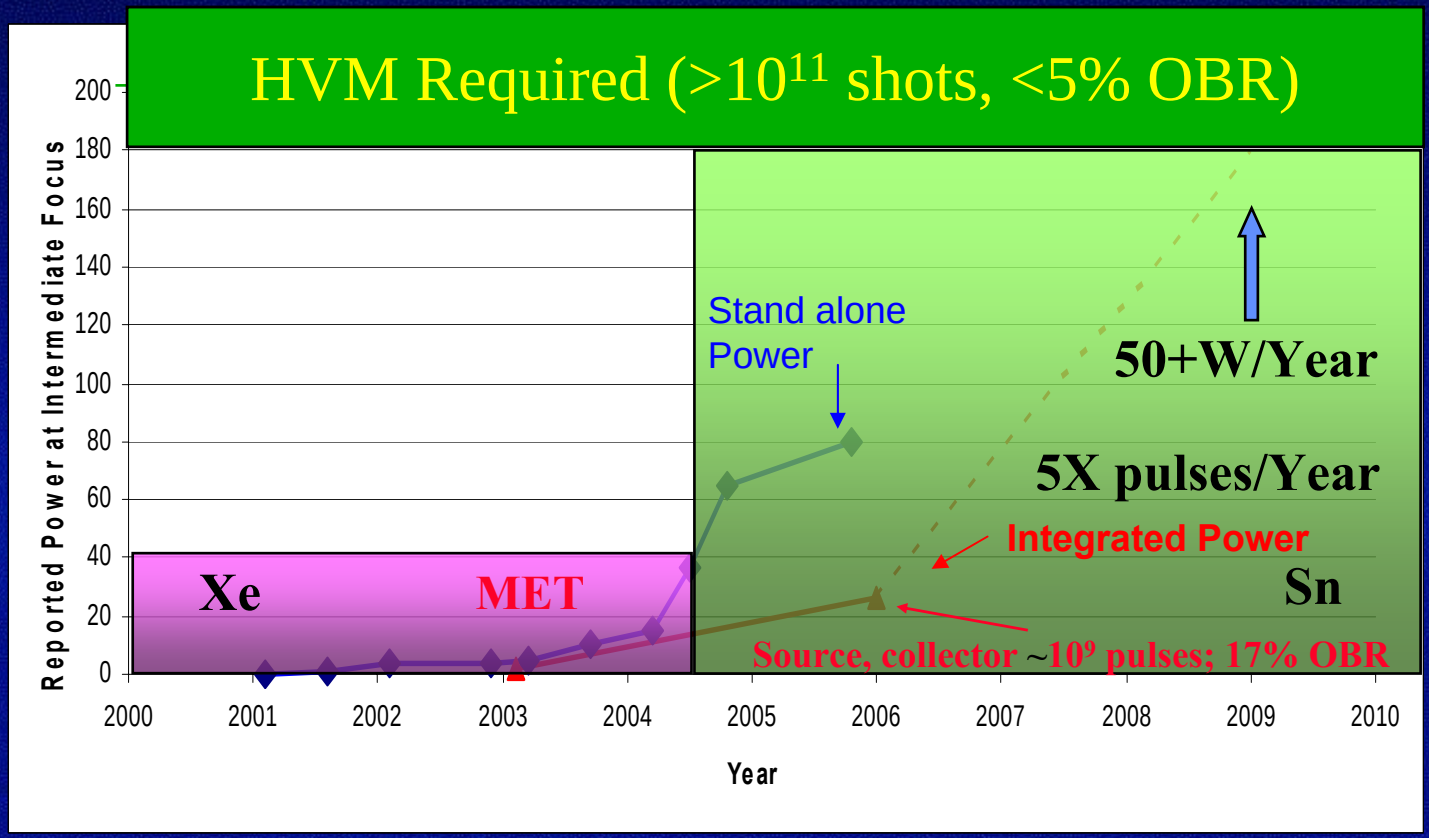
Next 10 Years - Dual λ Options

EUV Route – Source Power



Next 10 Years - Dual λ Options

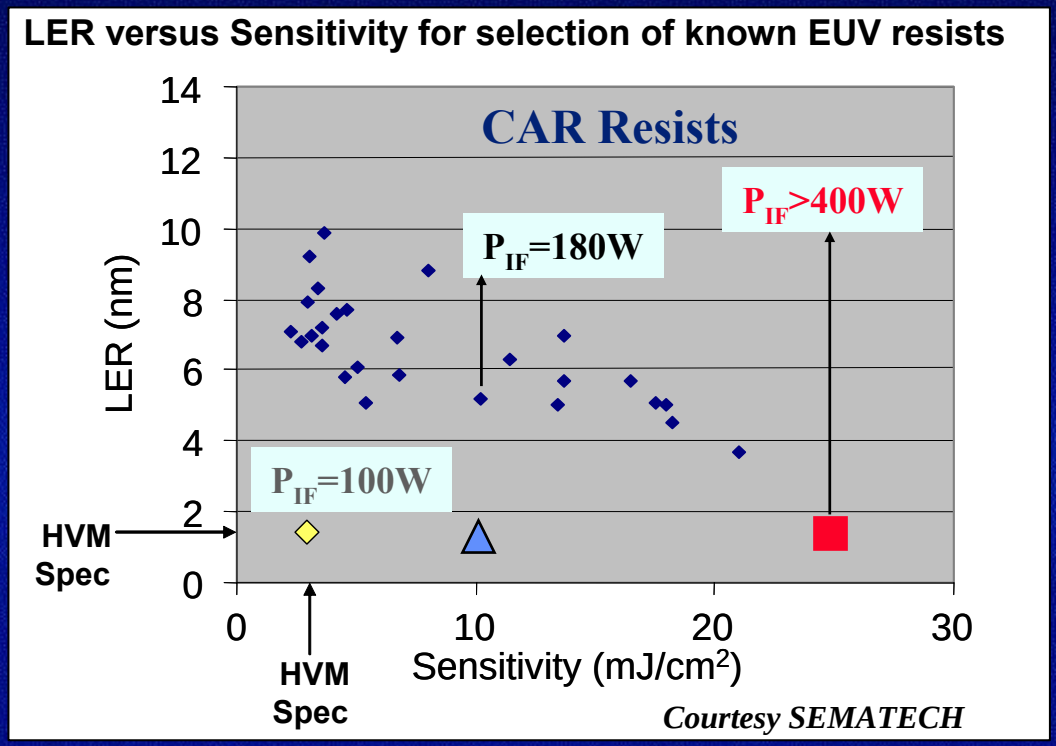
EUV Route – Source Power



Good Progress yet **whole is probably > then sum of the parts**

Next 10 Years - Dual λ Options

EUV Route – LWR/ Power



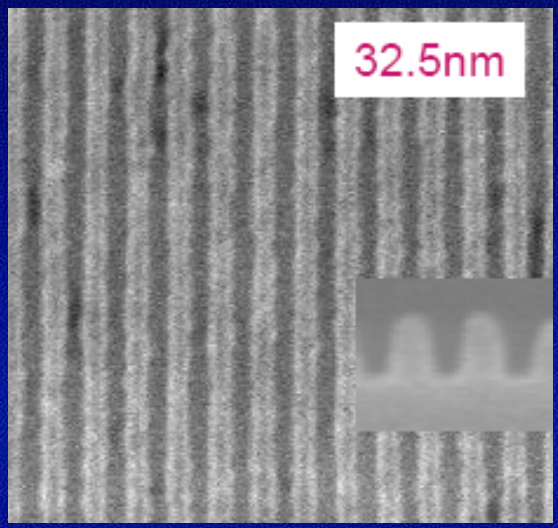
LWR>4nm might not be acceptable for 2011 devices.
Sn might not be able to deliver P_{IF}>>150-180W, required pulse number and collector components lifetime if extra power is needed to reduce LWR and OBR to needed level. Breakthrough needed!

Incremental improvements might not be sufficient .
Novel approach has to be developed to reduce EUV COO Risk.

Next 10 Years - Dual λ Options

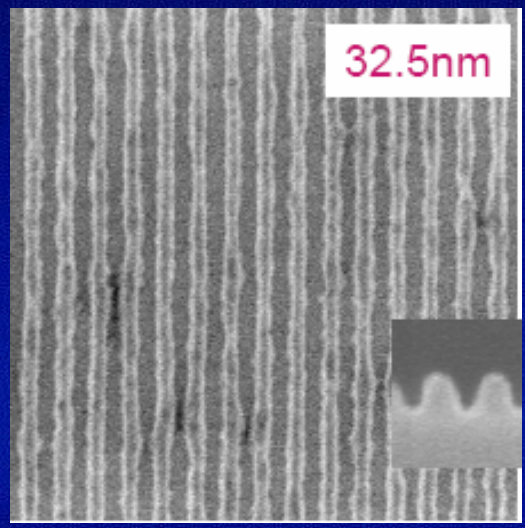
EUV Route – Resist

2004
EUV-6



Esize~11mJ/cm²
LER(3σ)=7.1nm

2005
EUV-25



E_{size}~7.5mJ/cm²
LER(3σ)=5.7nm

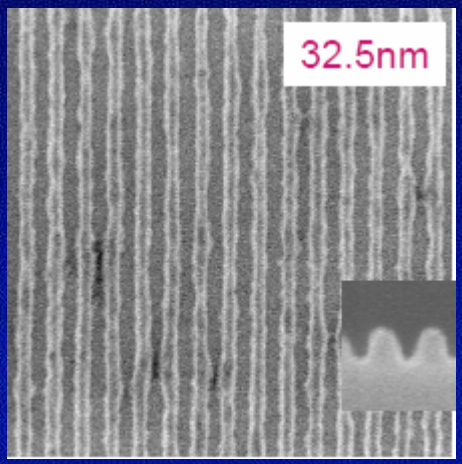
Roel Gronheid et al,
EUVL symposium, San Diego, November 8, 2005

Good Progress on pushing Resolution limits and LWR for high sensitivity CARS

Next 10 Years - Dual λ Options

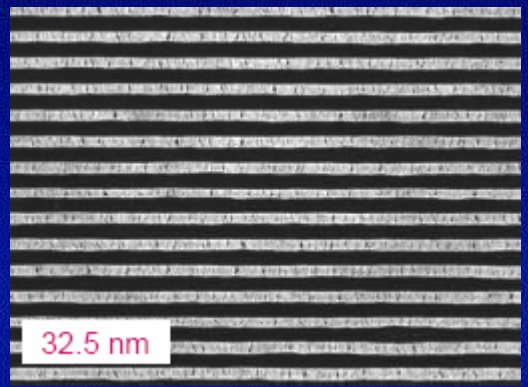
EUV Route – Resist

CAR – EUV-25



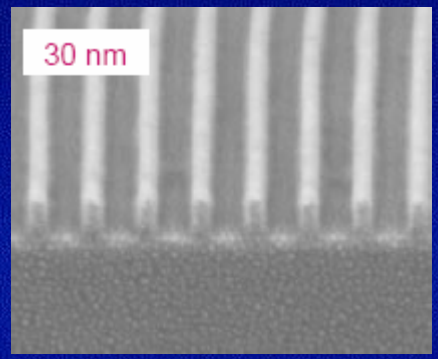
E_{size}~7.5mJ/cm2

PMMA



Esize~50mJ/cm2

PMMA

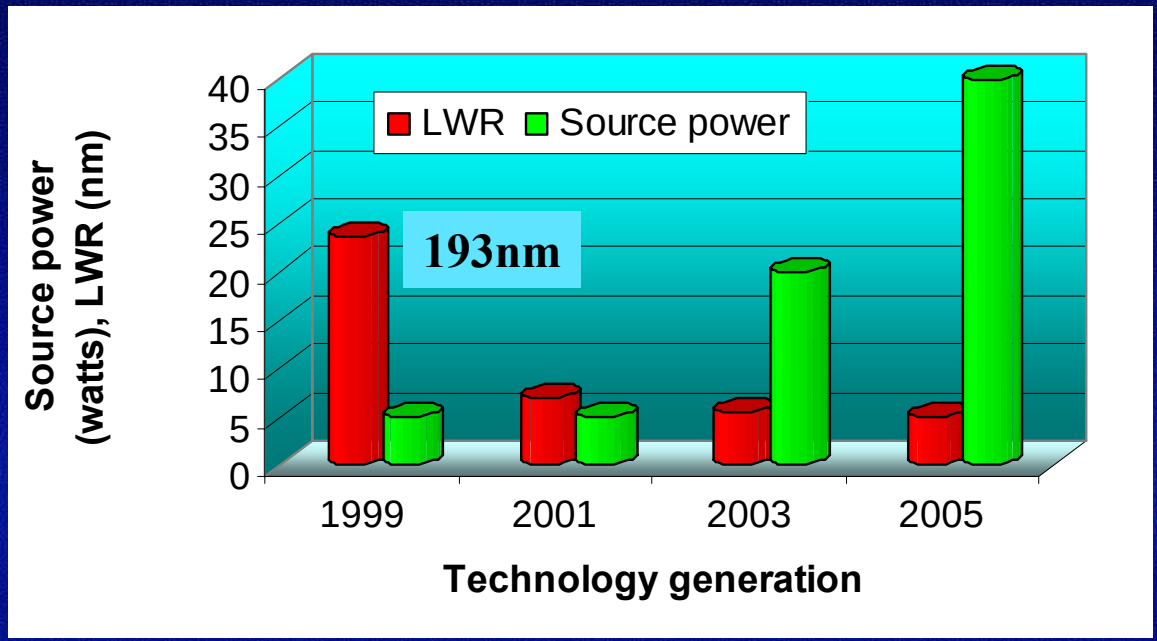


Roel Gronheid et al,
EUVL symposium, San Diego, November 8, 2005

Best Resolution in CAR is resist limited.
No CAR < 32nm half-pitch even with IL.
Critical issue for 2011 HVM.

Next 10 Years - Dual λ Options

EUV Route – Resist



>50 new formulations were tested every month to bring current 193nm resists performance.

Same or higher rate of learning necessary to enable required EUV resists performance.

Inexpensive, reliable, easy to maintain EUV Interference TOOL needed to enable breakthrough and fast learning at multiple locations involved in formulation and synthesis of EUV resists

Next 10 Years - Dual λ Options

193nm Route – it is here

HVM Year/Tool	k1 SE	Litho Challenge from Previous Generation	Availability Proof
2007 193/0.93	0.38	Evolutionary	2005
2009 193/0.93	0.29	New, RET	2006
193/1.20	0.37	New, Defects source, dry/wet OL	2006
2011 193/0.93DE	0.40	New, SE/DE methodology, OL	2007
193/1.35	0.29	New, Evolutionary if 193/1.2 in 2009	2008
2013 193/0.93DE	0.29	Evolutionary if 0.93DE in 2011	2008
193/1.20DE	0.37	Evolution if 193i,DE in 2009,2011	2008
2015 193/1.35DE	0.29	Depends on 2009-2013 choice	

Air and H_2O based 193 tools can support HVM through 2015+

"Airmens" vs "Submariners" every 2 years through 2013 HVM!

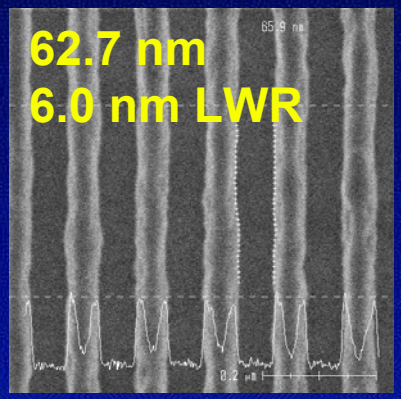
193nm Extension Enablers:

k1 = 0.29 Patterning

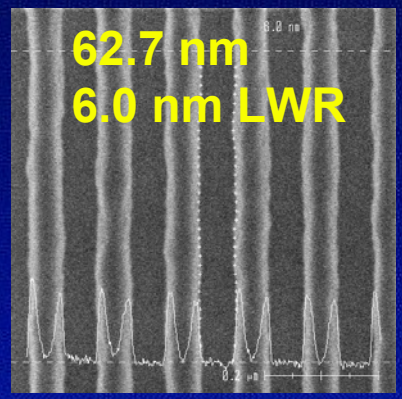
Dual Expose Methodology

k1=0.29 Patterning

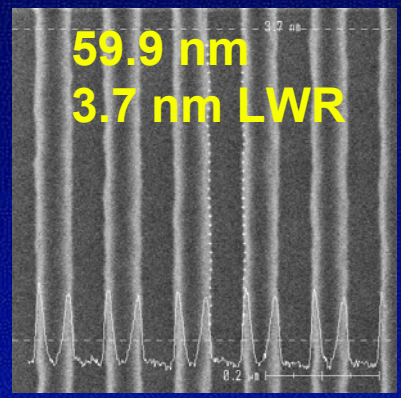
60nm space/line; 193nm/0.93NA; C-quad (Unpolarized), 6% EPSM



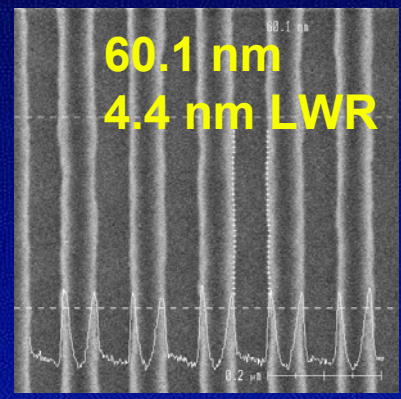
-F=- 0.15 um



F=- 0.10 um



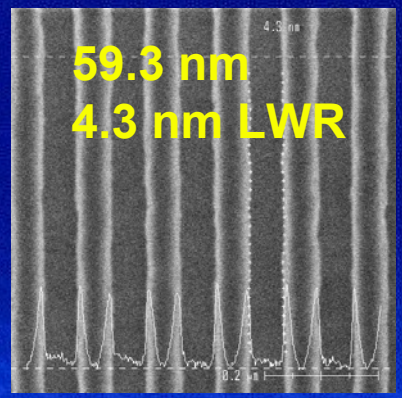
F=-0.05 um



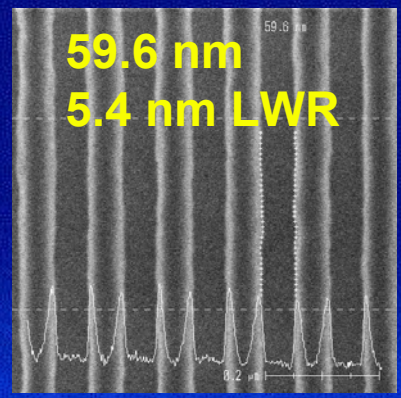
F=0.0 um

Commercial resist

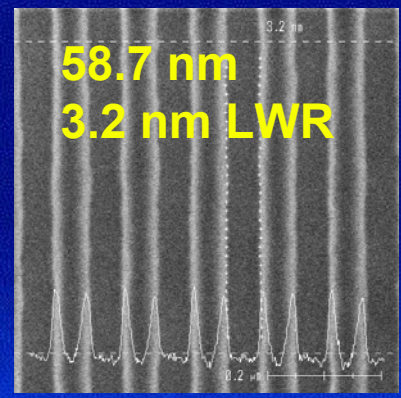
1:1 Dose=29mJ/cm^2



F=0.15 um



F=0.10 um



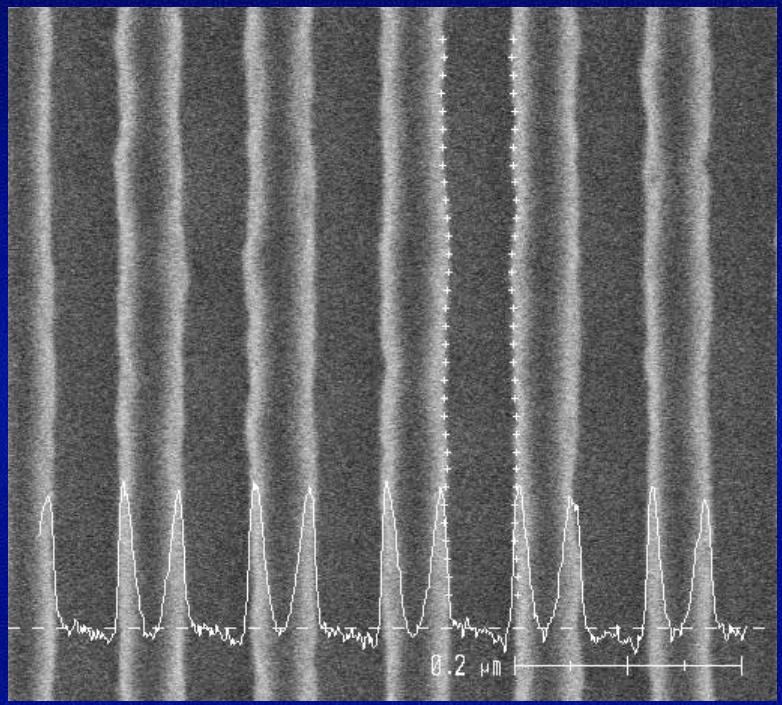
F=0.05 um

Data courtesy
C.Wallace/S.Sivakumar

k1 ≤ 0.29 Patterning

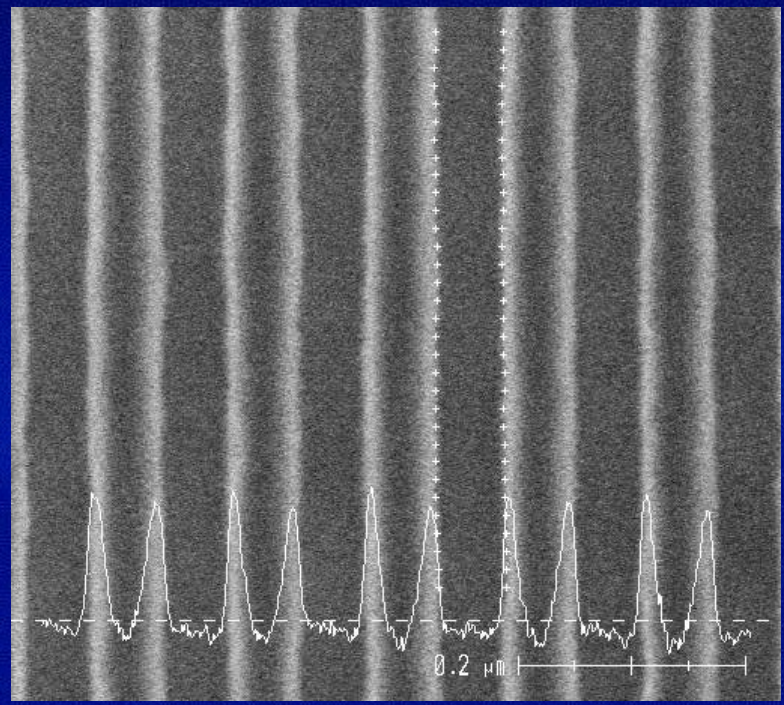
193nm/0.93NA; C-quad (Unpolarized), 6% EPSM

Pitch=115 nm (60/55 s/l)



Space CD= 60.0 nm
5.9 nm LWR

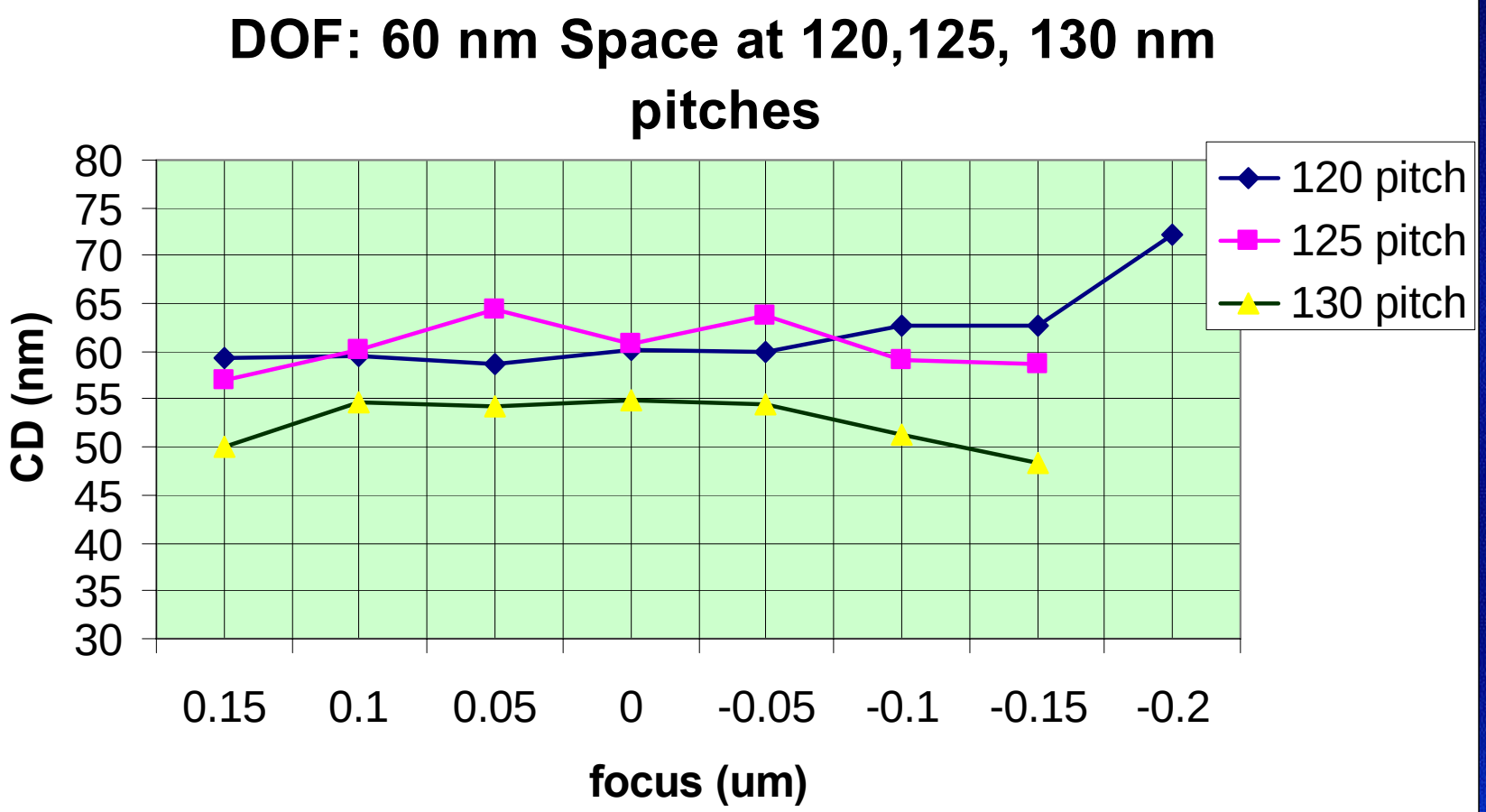
Pitch=120 nm (60/60 s/l)



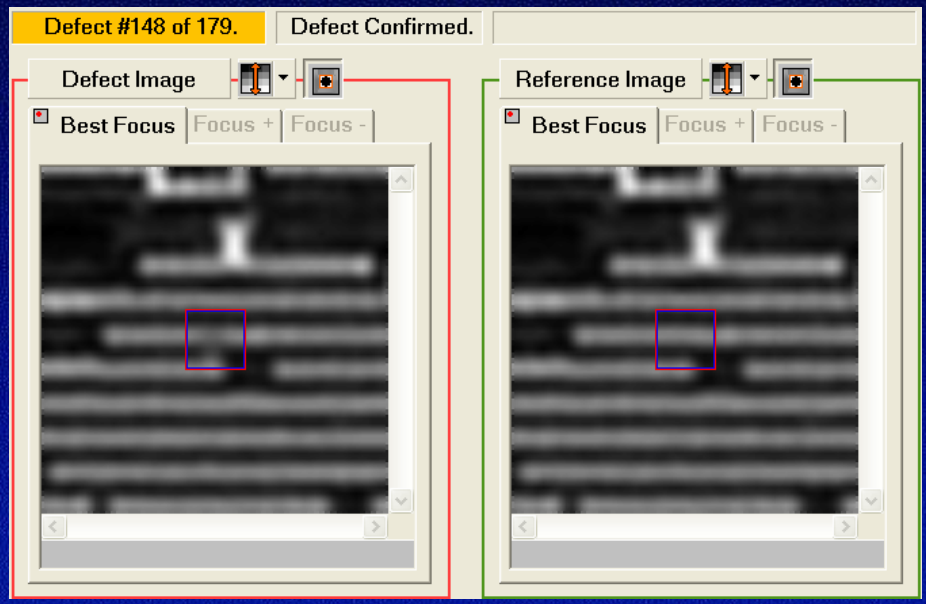
SpaceCD=60.1 nm (29mj/cm^2)
3.2 nm LWR (LER =1.6nm)

k1 ≤ 0.29 Patterning

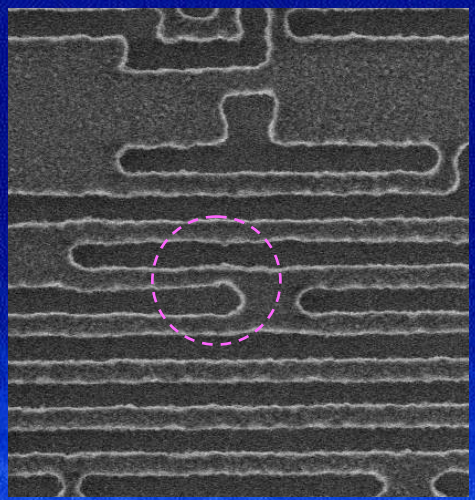
193nm/0.93NA; C-quad (Unpolarized), 6% EPSM



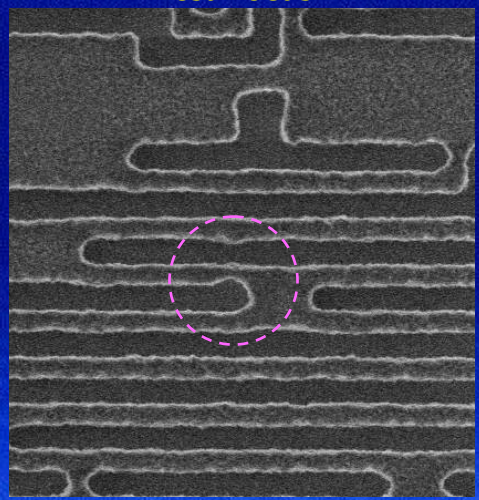
Aerial Image Based Mask Inspection



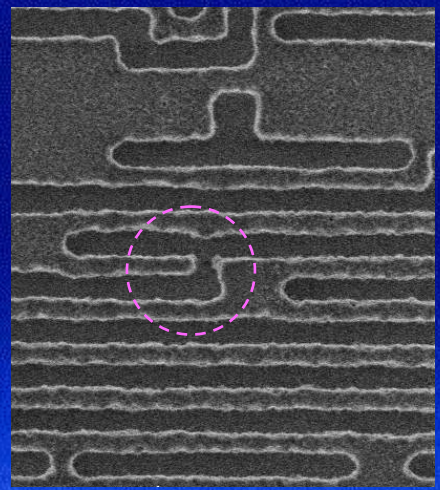
BF-0.125um



Best Focus



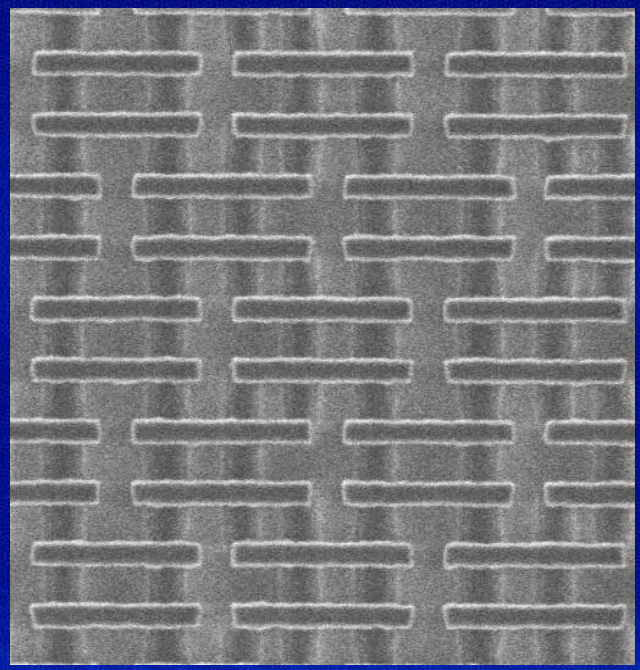
BF+0.125um



Dual Exposures

Dual Exposures are used by Logic & Memory makers in HVM already

Gate patterning with Alternating PSM for Logic and Core/Periphery patterning by Memory makers are better known examples of use of DE

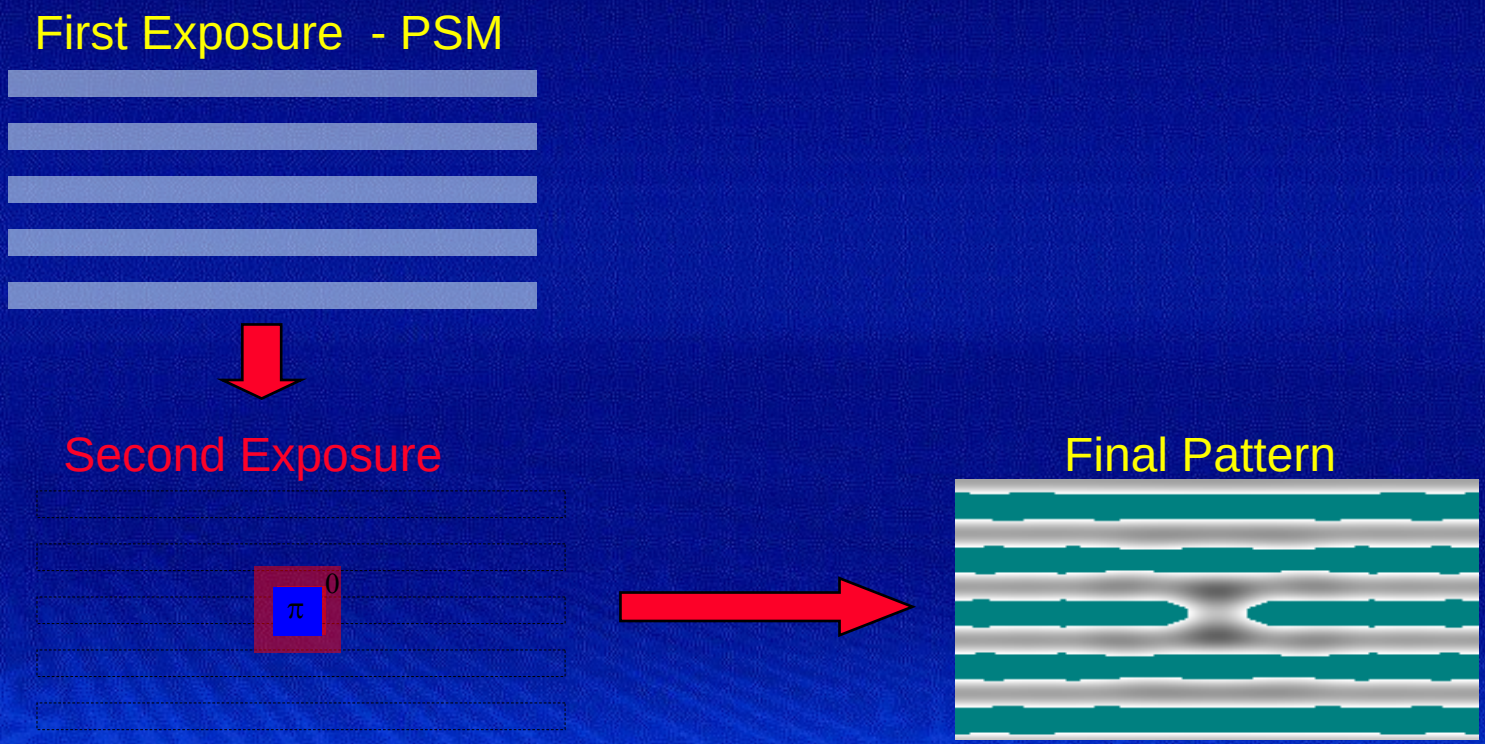


Intel 45nm node Gate Patterning, Dual Exposure for higher density

COOL Patterning

COmposite Optical Lithography

First exposure produced a "grating" in Negative resist using PSM. Second PSM exposure "plugged" the grating with 65nm node tool

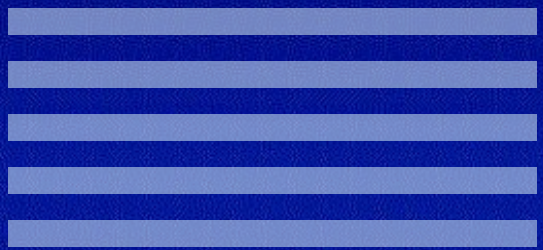


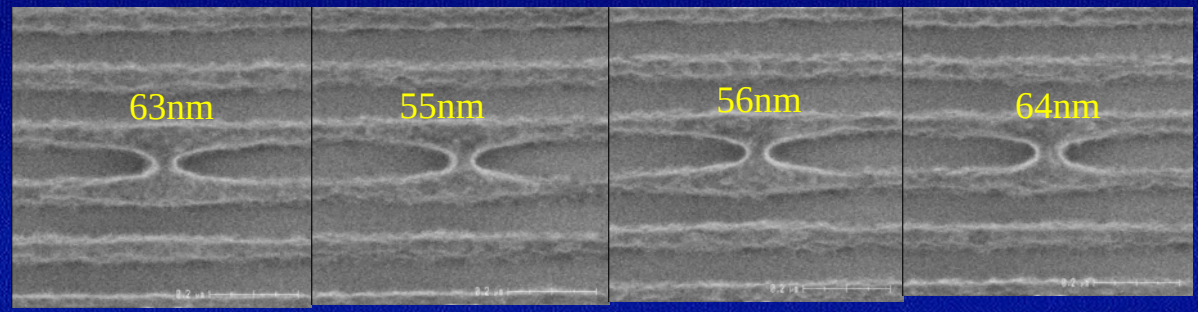
COOL Patterning

COmposite Optical Lithography

First exposure produced a "grating" in Negative resist using PSM. Second PSM exposure "plugged" the grating with 65nm node tool

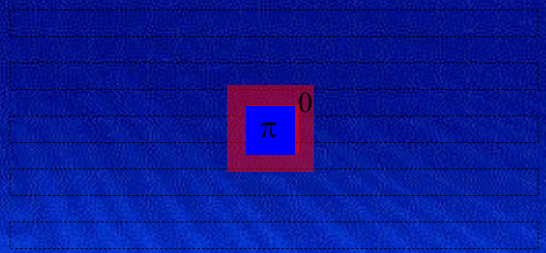
First Exposure - PSM



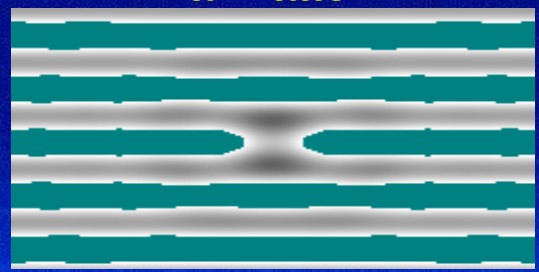


F=0.05um F=0.15um F=0.25um F=0.35um

Second Exposure



Final Pattern



Split and Shift Exposure

- Multiple publications on use of Dual Exposure to halve pitch with Split And Shift Exposures (SASE) starting from late 1980s.
- SASE patterning demonstrated, Key challenges identified:

Cost	≤ 2*SE Cost – common concern to all
Integration	Best approach is yet to emerge
CD Control	Require > 2X OL improvement for Mask and scanner
OL Control	Same as above

SASE Type	Masks	Resists	ARCs and HMs	E1- E2 bake/cure	Primary Feature	Half Pitch	Lambda NA	k1 SASE	Author
DLS	2	Resist1 Resist2(Si)	BARC A-Si HM SION HM C-HM	No	Line	45	193/0.68	0.16	C.Noelscher et al MNE 2005
ORAMEX	1(2)	1	BARC	No	L, S	125	248/0.60	0.3	M.Neisser A.Molless SPIE 1998
DLS	2	2 1	BARC C-HM	UV-Cure Bake	C/H	75	193/0.78	0.3	H.Nakamura et al. JM3 '05
PAU/PAC	2	Resist1 Resist2 (Alcohol)	EEP DBARC	UV-Cure Bake	C/H	70	193/0.85	0.31	D.C.OweYang et al. SPIE 2005

SASE - New Materials Needed

- **SASE complexity and cost is detriment to its use in HVM.**
- **SASE might become attractive for development and high volume manufacturing considerations if:**

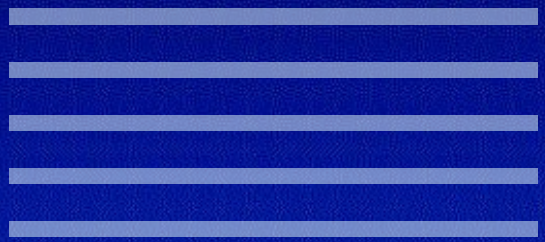
a) SE alternatives are high risk/high cost
b) Low cost/Low complexity SASE proposed

Yet to be developed photosensitive materials might hold the key to economical SASE solution

SASE (Sci-Fi)

"OSOM" Resist/COOL (1 Resist /1 Mask):

1st IL Expose
Latent image



"Out of Sight Out of Mind"

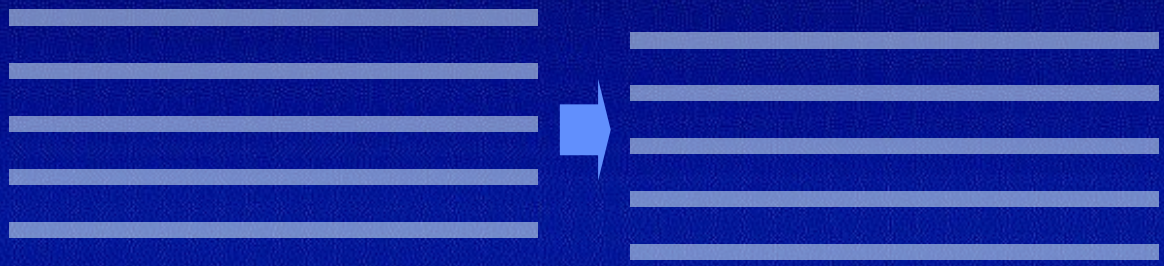
Resist with no memory of
partial exposure
(phase change or suchlike)

SASE (Sci-Fi)

"OSOM" Resist/COOL (1 Resist /1 Mask):

1st IL Expose
Latent image

2nd IL Expose P/2 shift
Latent image



"Out of Sight Out of Mind"

Resist with no memory of
partial exposure
(phase change or suchlike)

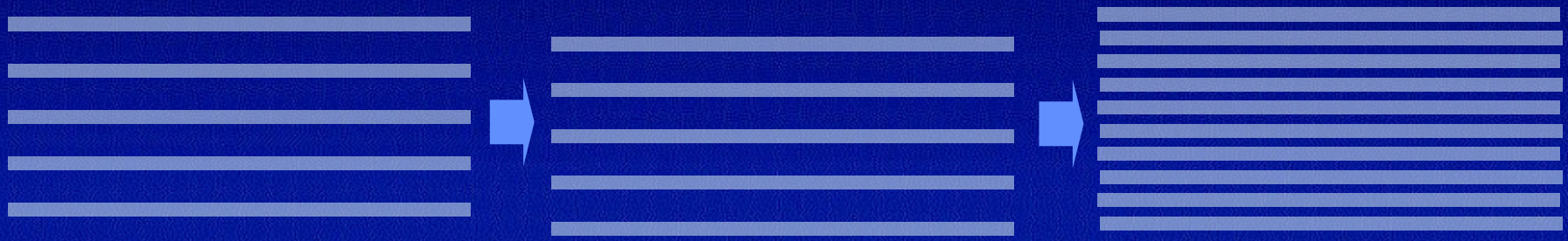
SASE (Sci-Fi)

"OSOM" Resist/COOL (1 Resist /1 Mask):

1st IL Expose
Latent image

2nd IL Expose P/2 shift
Latent image

Resulting
Latent image



"Out of Sight Out of Mind"

Resist with no memory of
partial exposure
(phase change or suchlike)

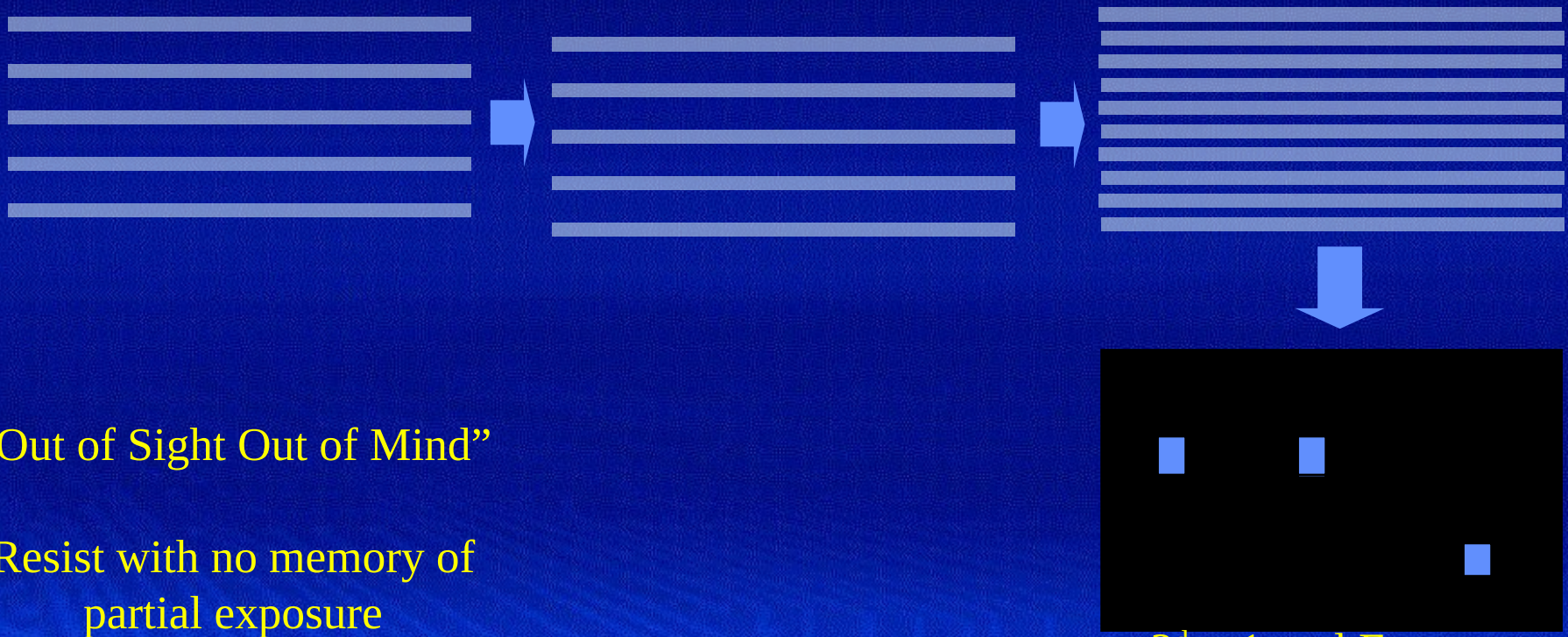
SASE (Sci-Fi)

"OSOM" Resist/COOL (1 Resist /1 Mask):

1st IL Expose
Latent image

2nd IL Expose P/2 shift
Latent image

Resulting
Latent image



"Out of Sight Out of Mind"

Resist with no memory of
partial exposure
(phase change or suchlike)

3d n-1 tool Expose
Latent image

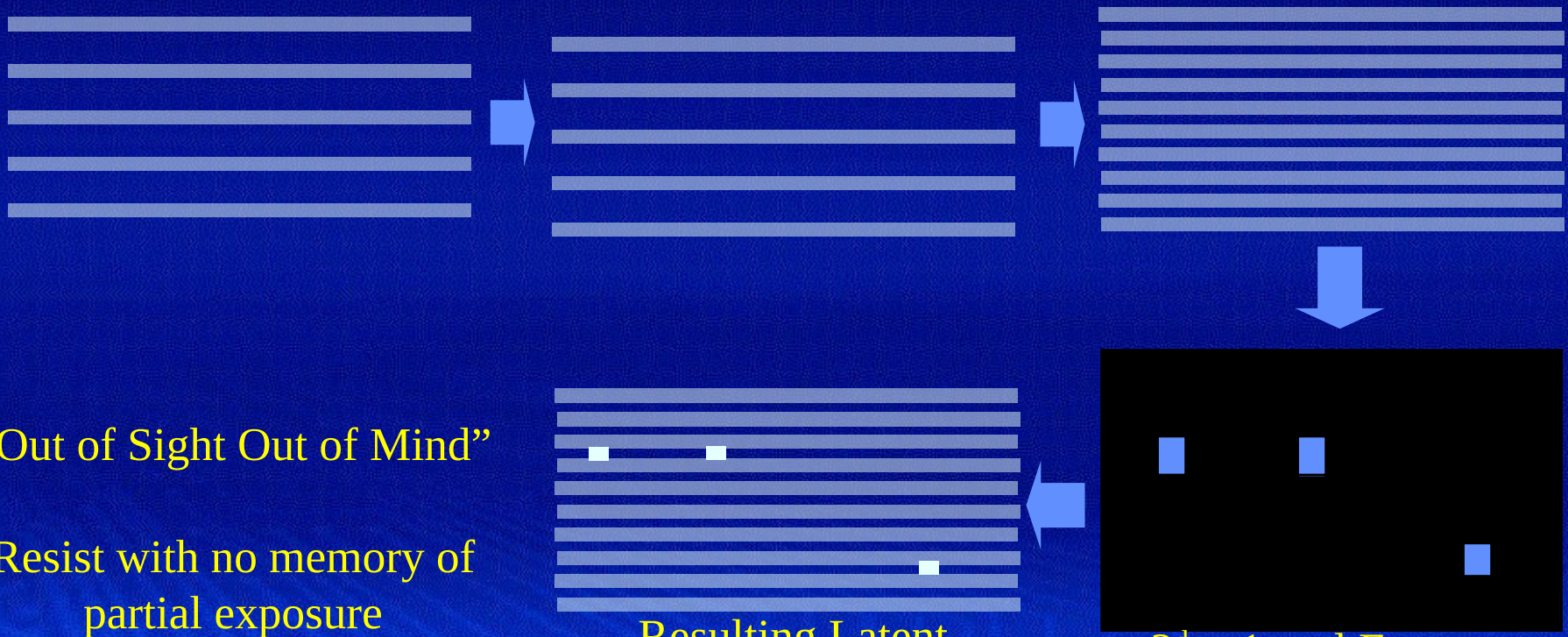
SASE (Sci-Fi)

"OSOM" Resist/COOL (1 Resist /1 Mask):

1st IL Expose
Latent image

2nd IL Expose P/2 shift
Latent image

Resulting
Latent image



"Out of Sight Out of Mind"

Resist with no memory of
partial exposure
(phase change or suchlike)

Resulting Latent
image

3d n-1 tool Expose
Latent image

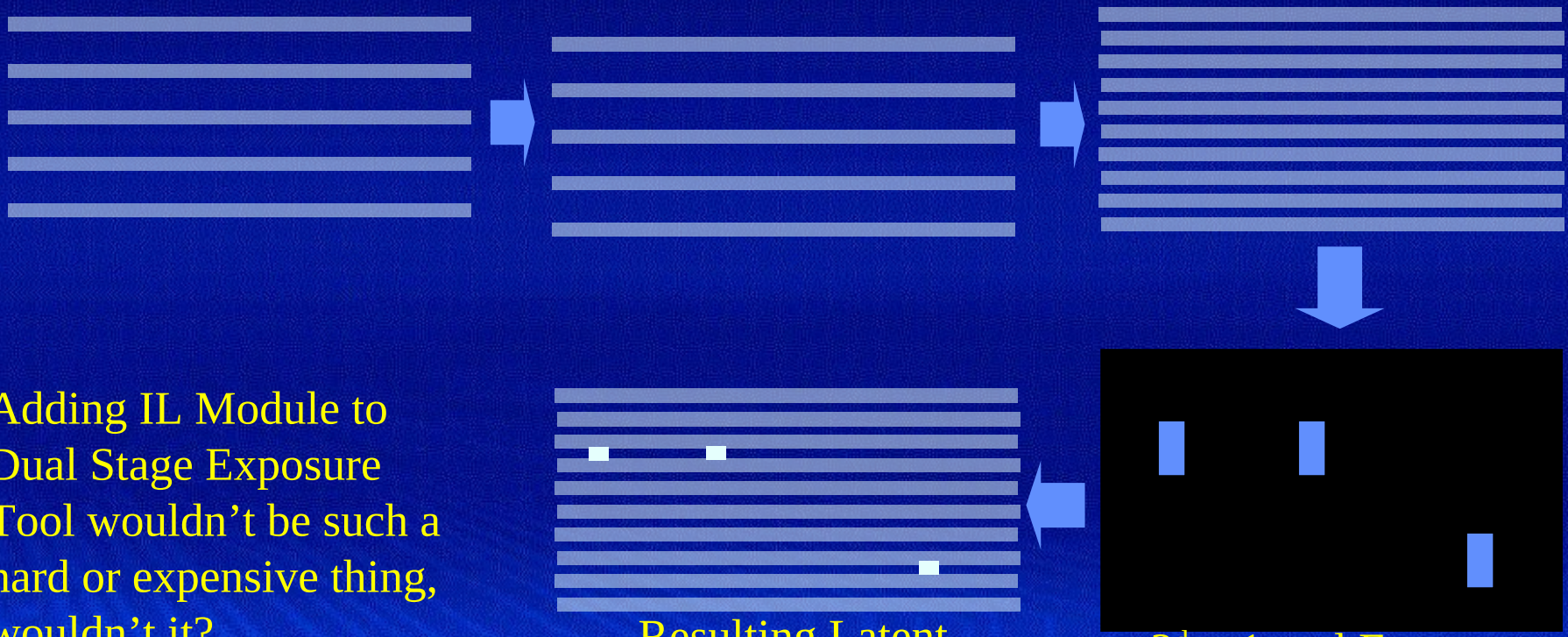
Cheap Dual Exposures (Sci-Fi)

OSOM COOL:

1st IL Expose Latent image

2nd IL Expose Latent image

Resulting Latent image



Adding IL Module to Dual Stage Exposure Tool wouldn't be such a hard or expensive thing, wouldn't it?

Resulting Latent image

3d n-1 tool Expose Latent image

Cheap Dual Exposures (Sci-Fi)

OSOM COOL

1st IL Expose Latent image

2nd IL Expose Latent image

Resulting Latent image

16nm hp with Gen II fluid at $k1_{SE}$=0.26

Adding IL Module to Dual Stage Exposure Tool wouldn't be such a hard or expensive thing, wouldn't it?

Resulting Latent image

3d n-1 tool Expose Latent image

SASE vs SE COO

What if TPT limits for Air/Liquid systems are different?

Hypothetical case study

Scan Speed Limiter	193 Air	193 H2O	193 GENII
Photons / Resist Speed	1200	1200	1200
Inertia / Stage Mechanics	1000	1000	1000
Fluid Handling / Defects	-	500	400
Productivity Factor	1	0.5	0.4

Hypothetical Values in mm/s

Tool vendors should educate industry and customers on respective platforms limits for early roadmap alignment and possible simplification.

Decisions, Decisions…

Airmen vs Submariners 2009

HVM Year/Tool	**k1** SE	Litho Challenge from Previous Generation	Availability Proof
2009 193/0.93	**0.29**	**New, RET**	**2006**
193/1.20	**0.37**	**New, Defects sources, dry/wet OL**	**2006**

Airmen

To score need:

- **k1=0.29 Patterning**
- **CD Control - same as wet**
- **Better OL**
- **Better COO**

Submariners

To score need:

- **Defects - Same as dry**
- **Superior CD Control**
- **Wet/dry OL = to dry/dry**
- **Better COO**

Airmen and Submariners 2011 vs Astronauts

HVM Year/Tool	k1 SE	Litho Challenge from Previous Generation	Availability Proof
2011 193/0.93DE	0.40	New. SE/DE methodology, CD/OL	2008
193/1.35	0.29	Evolutionary if 193/1.2 in 2009	2008
13.5/0.25	0.78	New, Defects, TPT/LER; EUV/193 OL	2009

Airmen

To score need:

- Same Defects level
- DE split CAD
- Same CD Control
- DE OL = SE OL
- Equal COO

Submariners

To score need:

- Same Defects level
- k1=0.29 Patterning
- Same CD Control
- Wet/dry OL= dry/dry
- Better COO

Astronauts

To score need

- Same Defects level
- Uptime >0.9*193nm
- Better CD Control
- EUV/dry OL=dry/dry
- Better COO

Airmen and Submariners 2013 vs Astronauts

HVM Year/Tool	**k1** SE	Litho Challenge from Previous Generation	Availability Proof
2013 193/0.93DE	**0.29**	**Evolutionary if 0.93DE in 2011**	**2008**
193/1.20DE	**0.37**	**Evolution if 193i,DE in 2009,2011**	**2009**
13.5/0.35	**0.78**	**Evolutionary if EUV in 2011**	**2011**

Airmen

To score need:

- **DE split CAD**
- **k1=0.29 Patterning**
- **CD Control =wet**
- **OL Control =wet**
- **Better COO**

Submariners

To score need:

- **DE split CAD**
- **Same Defects level**
- **Better CD Control**
- **Wet/dry OL = to dry/dry**
- **Better COO**

Astronauts

To score need

- **Uptime >0.9*193nm**
- **Same Defects level**
- **Better CD Control**
- **EUV/dry OL=dry/dry**
- **Better COO**

Submariners vs Astronauts 2015

HVM Year/Tool	**k1** SE	Litho Challenge from Previous Generation	Availability Proof
2015 193/1.35DE	**0.29**	**Depends on 2009-2013 choice**	**2012**
13.5/0.35	**0.54**	**NA=0.35 might not be enough**	**2012**

Submariners

To score need:

- **DE split CAD**
- **k1=0.29 Patterning**
- **Better CD Control**
- **Equal OL Control**
- **Better COO**

Astronauts

To score need

- **Uptime >0.9*193nm**
- **Same Defects level**
- **Better CD Control**
- **Equal OL Control**
- **Better COO**

Astronauts vs Airmen and Submariners

- EUV have to lift off, orbit Fab couple of times and land successfully to end the games.
- Currently used COO models and expected process benefits (comparable COO, k1>0.70) favor Astronauts provided pellicless patterning can be mastered at least 1.5 years before HVM.
- The earliest Astronauts will be ready to play the better – to realize the benefit of this promise.

Let the best man win!

Summary

- Multiple paths exist to continue Moore's Law on 2 year cycle for next 10-12 years.
- Intel R&D efforts and resources are used to establish credible ArF and EUV solutions for that time.
- Contenders for every node have to demonstrate proof of availability for all components at (HVM-1.5) Years.
- Final selection for every node will be based on Proof of availability, Process performance and expected COO.
- Extra effort will be required to take Air, Liquid and Vacuum based Lithography to their ultimate productivity.
- Novel photosensitive materials needed to enable most cost effective EUV and SAXE solutions

Thank you for attending

Copy of presentation can be downloaded from URL:

www.intel.com/technology/silicon